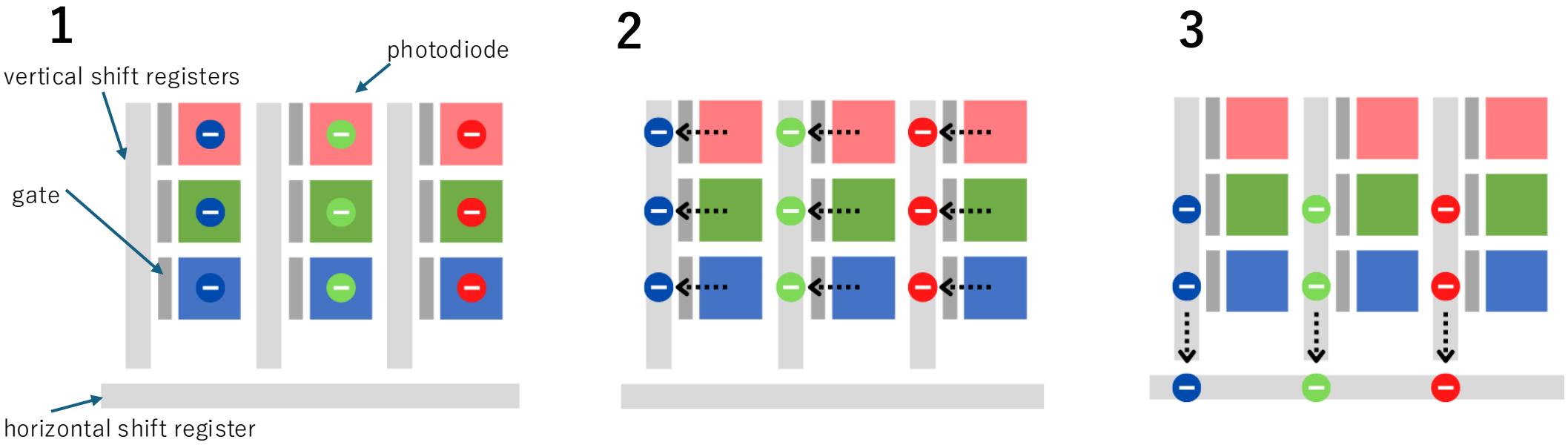
Mclean seminar sec.7.2.2-7.3.6

2024/09/27

M1 Kensho Tanaka

7.2.2 charge-coupling and clocking

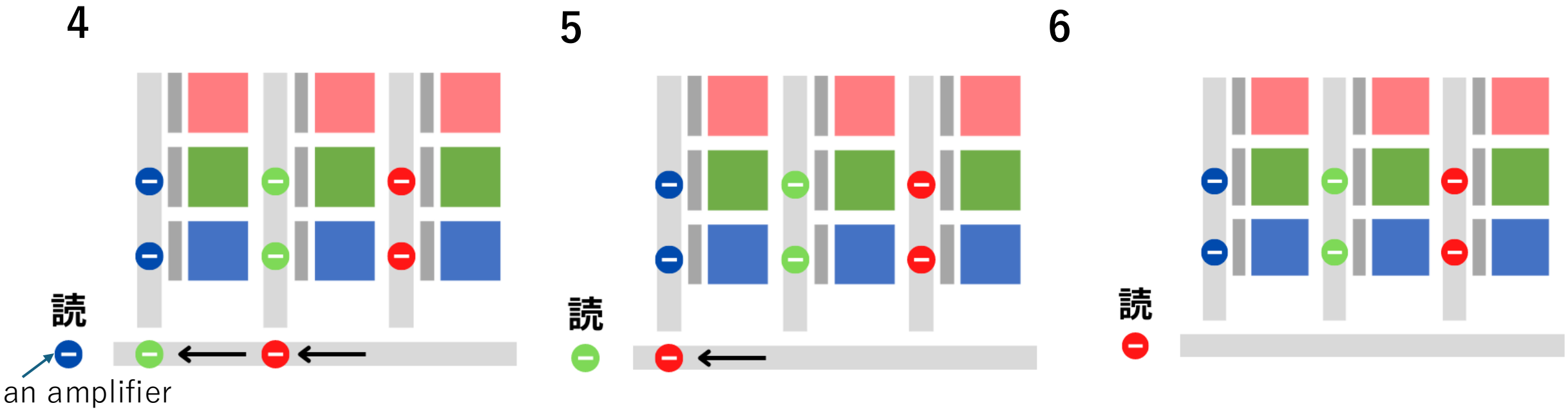
- **Jerry Kristian and Morley Blouke** first pointed out that taking a picture with a CCD is a bit like measuring the rainfall over a rather large plantation.



1. accumulate the electrons in a photodiode caused by entering photon
2. shift the electrons to the vertical shift registers
3. vertically transfer the electrons by one pixel

(https://semi-journal.jp/basics/device/image-sensor/ccd-cmos.html)

7.2.2 charge-coupling and clocking

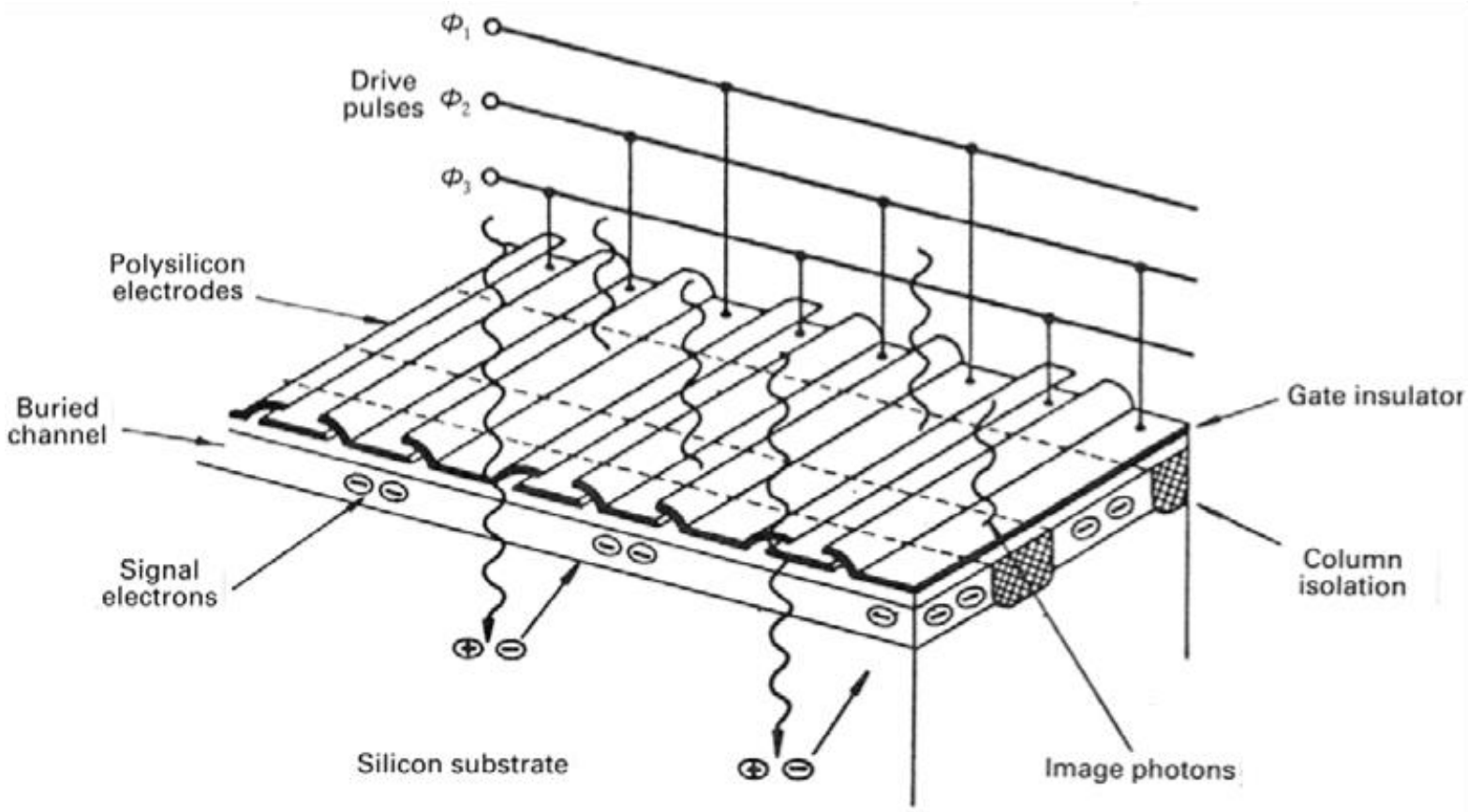


4. 5. 6. horizontally transfer electrons one by one along the horizontal shift register

(https://semi-journal.jp/basics/device/image-sensor/ccd-cmos.html)

7.2.2 charge-coupling and clocking

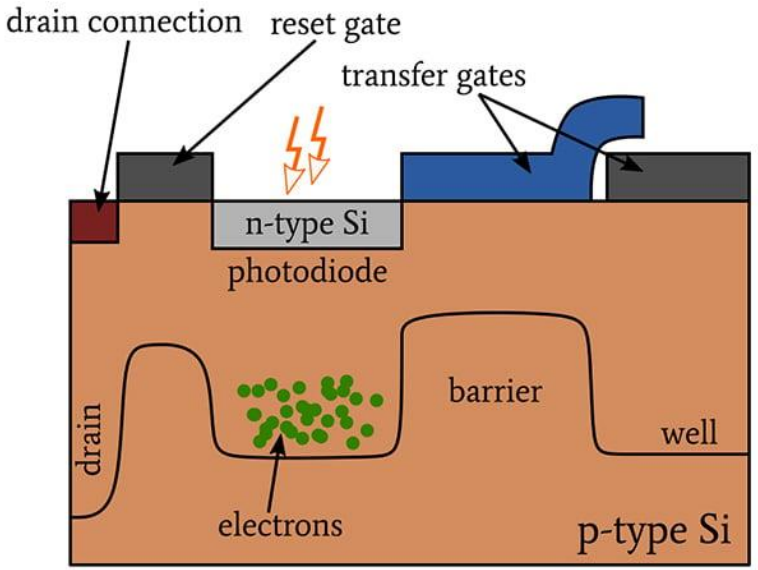
- **a “three-phase” structure**
- semiconductor silicon is covered with a thin electrical insulating layer of silicon oxide on top of which are placed **three sets of metal electrode strips.**

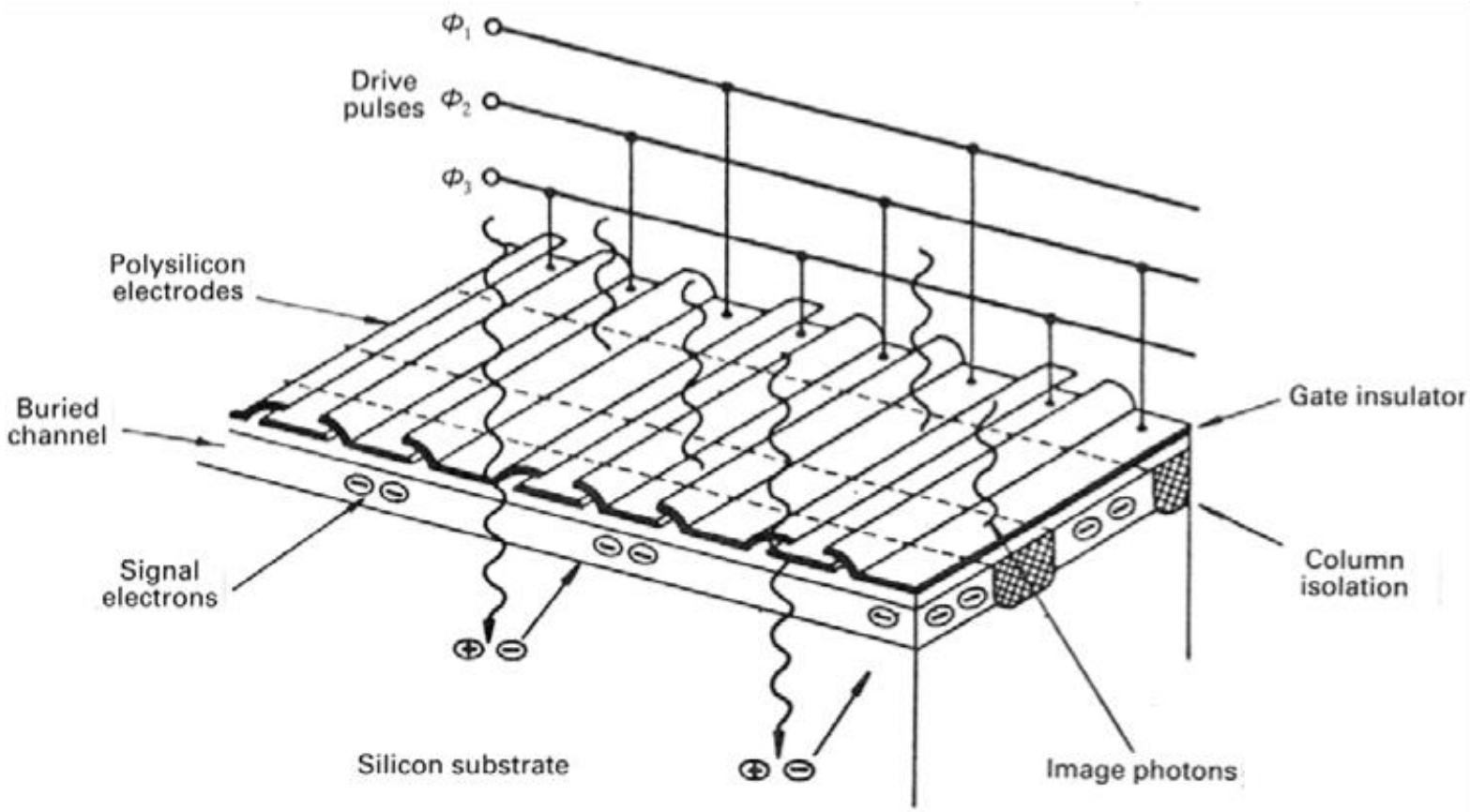


- One of the three strips is set to a more positive voltage than the other two,
  - the depletion region or bucket forms under this one, and where the electrons accumulate.

7.2.2 charge-coupling and clocking

- We have created two walls of the well.
  - by heavily doping the silicon crystal with a certain impurity
  - create a very narrow channel which totally obstructs any movement of charge along the length of the electrode.
  - channel stops



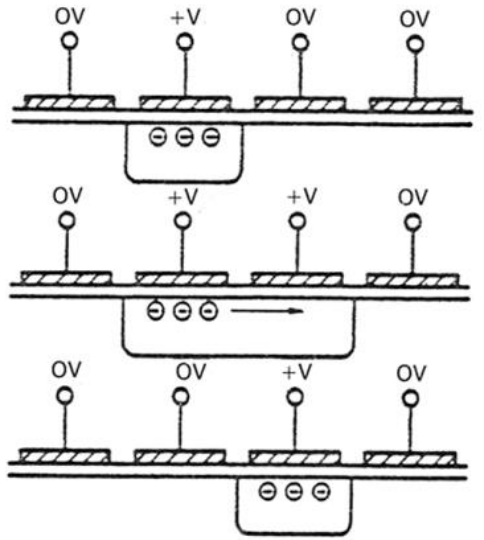


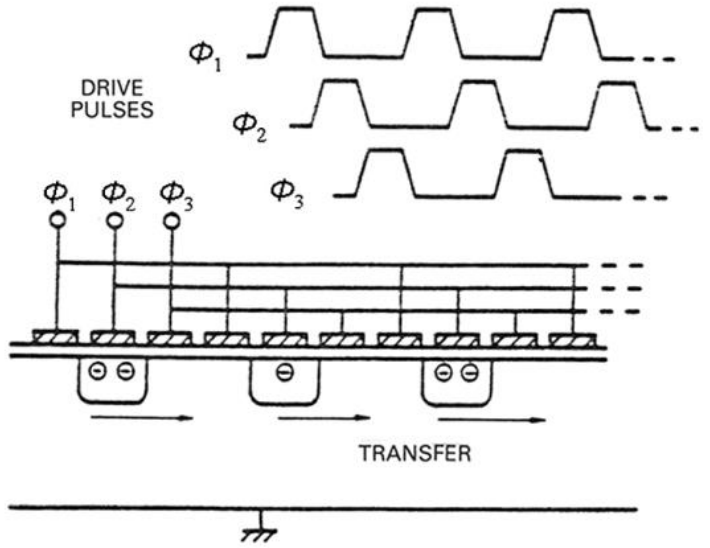
https://www.allaboutcircuits.com/technical-articles/understanding-the-structure-and-functionality-of-ccds/

7.2.2 charge-coupling and clocking

- To transfer charge from under one electrode to the area below an adjacent electrode, raise the voltage on the adjacent electrode to the same value as the first one.
- Transfer can be in either direction.

- The process of raising and lowering the voltage can be repeated over and over and is known as clocking.



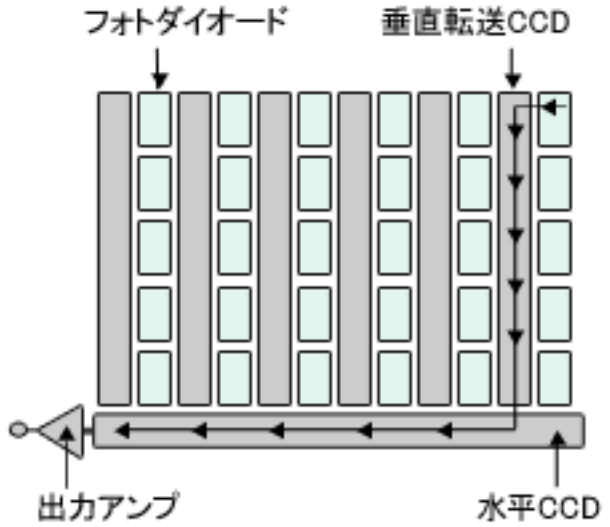


a timing waveform

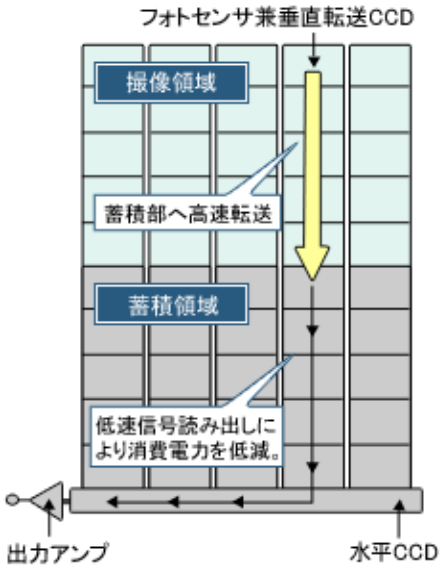
7.3 CCD CONSTRUCTIONS

7.3.1 Interline and frame transfer CCDs

- “interline” transfer
  - charges are moved **sideways** at high speed by one pixel to be relocated in a pixel which is shielded from light by an extra overlying strip of opaque metal.
  - The charges are then coupled **lengthways** to transfer down the shielded column.
  - charge-coupling transfer is very fast



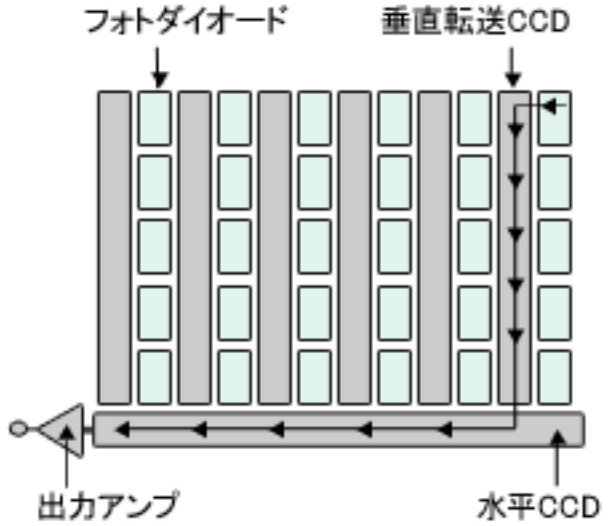
- ”frame” transfer
  - There are no blind spots in the imaging area.
  - instead a duplicate area, contiguous with the first, is covered by an opaque mask.
  - The transfer rate for readout is a little faster than the permitted “dwell time” on the image scene.
  - whereas **the image-to-storage rate is extremely high** to minimize blurring due to the illumination which is still present.

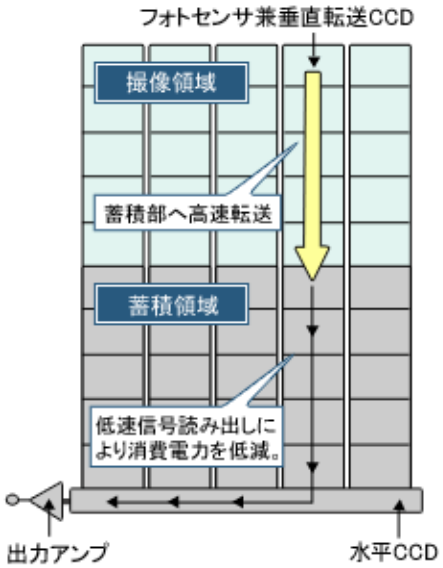


https://jp.sharp/products/device/technology/ic/ccd_cmos/kind/index.html

7.3.1 Interline and frame transfer CCDs

- frame transfer CCDs are best suited to astronomical applications, especially as the mask covering the storage area can be removed to yield a CCD of twice the original size.
- Blurring of the optical scene during readout is not a problem in astronomical applications because a light-tight electronically controlled shutter can be used to block off the incoming illumination.

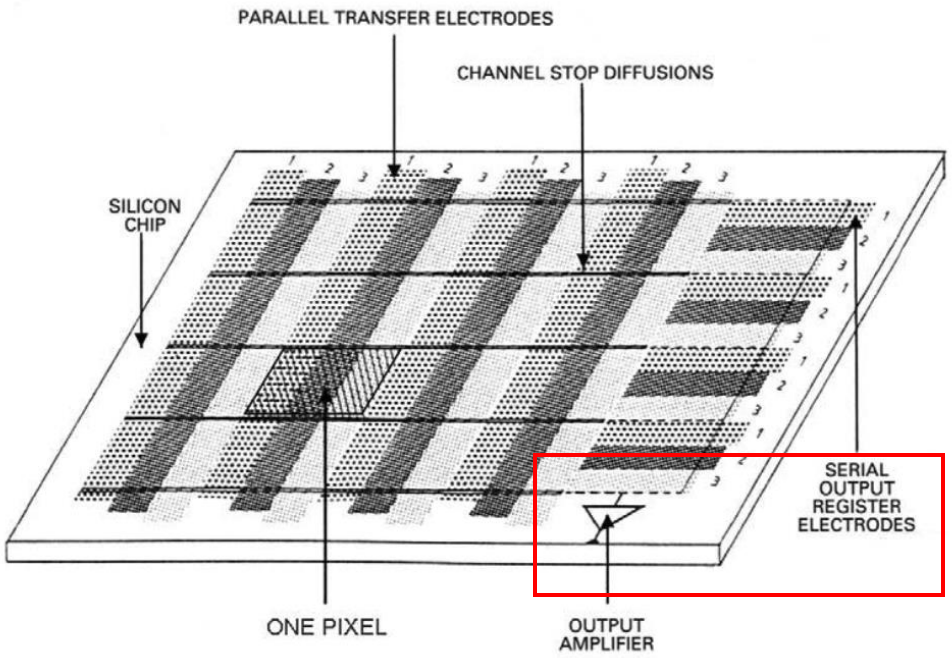




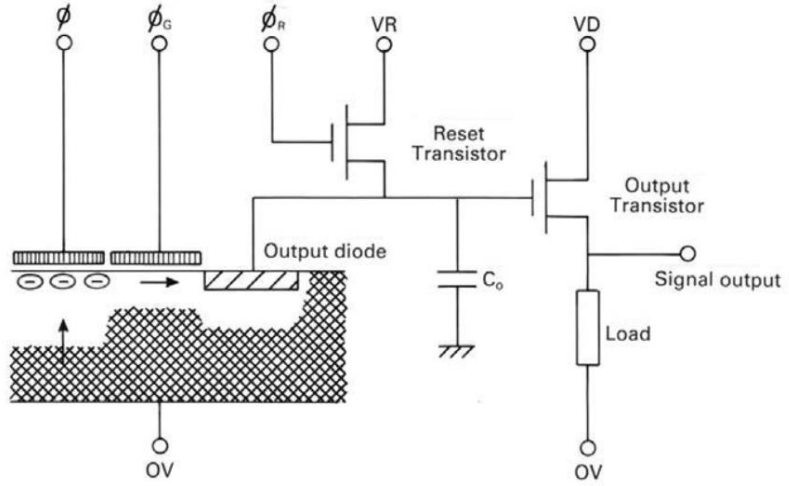
https://jp.sharp/products/device/technology/ic/ccd_cmos/kind/index.html

7.3.2 CCD outputs

- an “output register”
  - has electrodes arranged at right angles to the main area of the CCD, like the collection conveyer belt
  - transfer charge horizontally rather than vertically
  - called a “serial register”
  - the main area of the CCD is called the parallel register

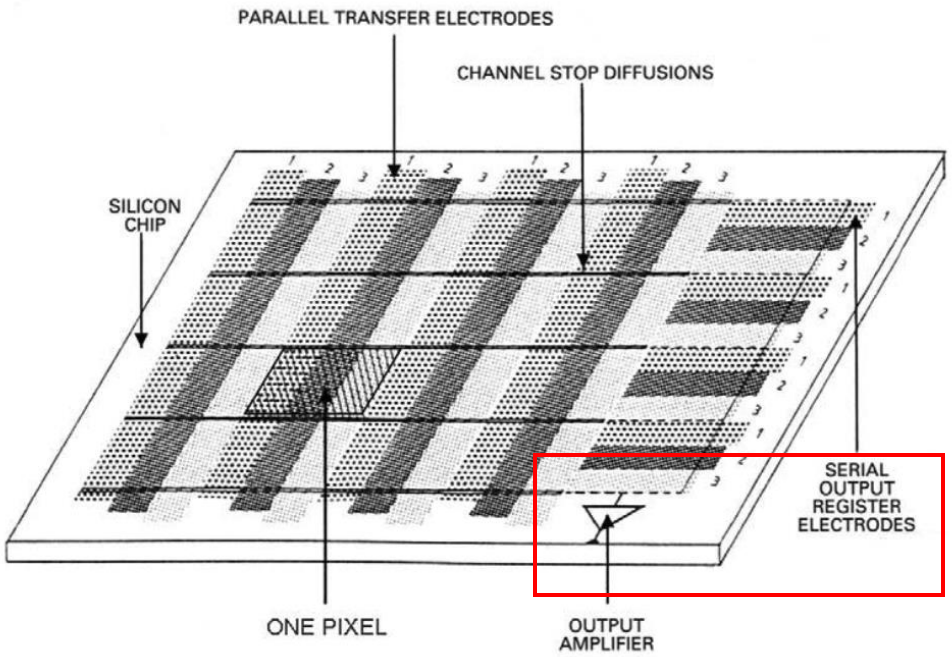


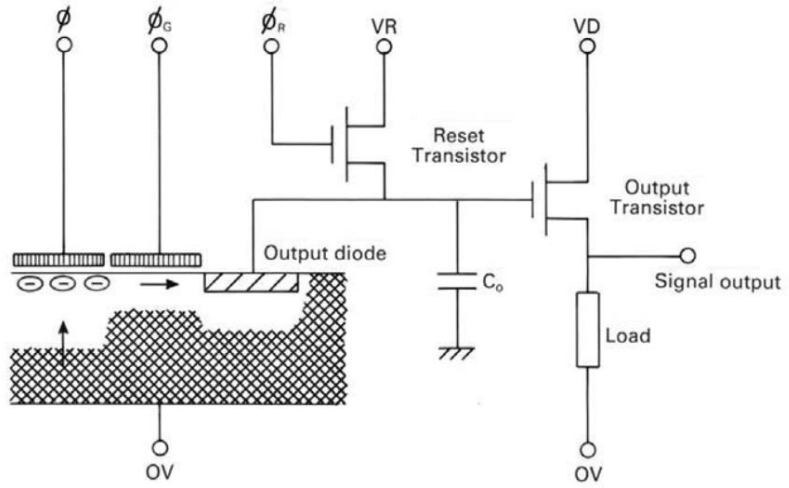
- The lower figure displays an electrical schematic of the circuit at the end serial register.



7.3.2 CCD outputs

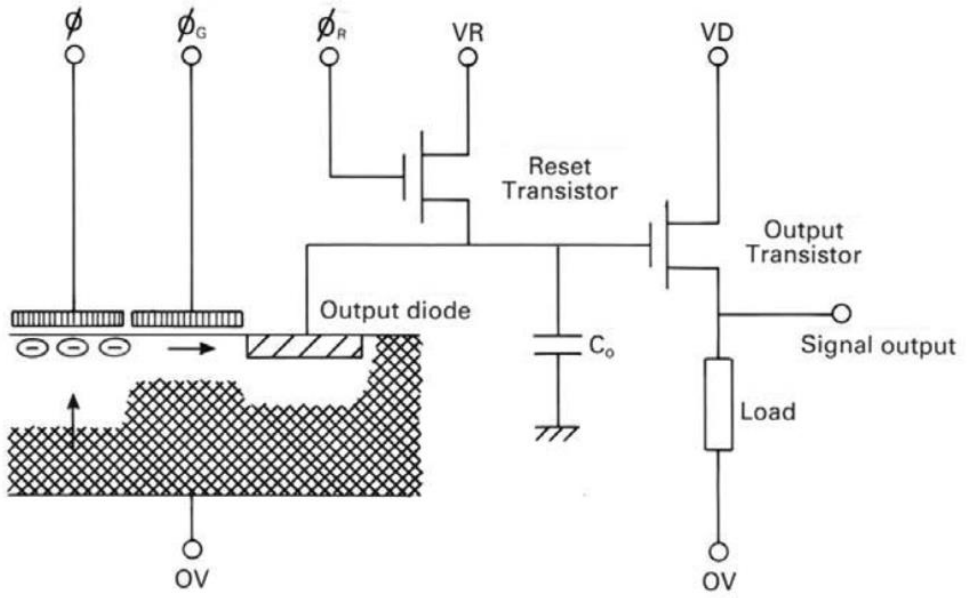
- A complete clocking sequence
  1. A vertical shift of the entire image scene by one pixel. This delivers a row of charge to the output register.
  2. A horizontal shift through all the pixels in the output register. This delivers each charge in that row to the output amplifier, one pixel at a time, where the charge can be detected and converted to a voltage which can be measured and recorded.
  3. Another vertical transfer to deliver the next row in the image to the serial register.
  4. Another horizontal transfer to move all the charges in the new row to the output.





7.3.2 CCD outputs

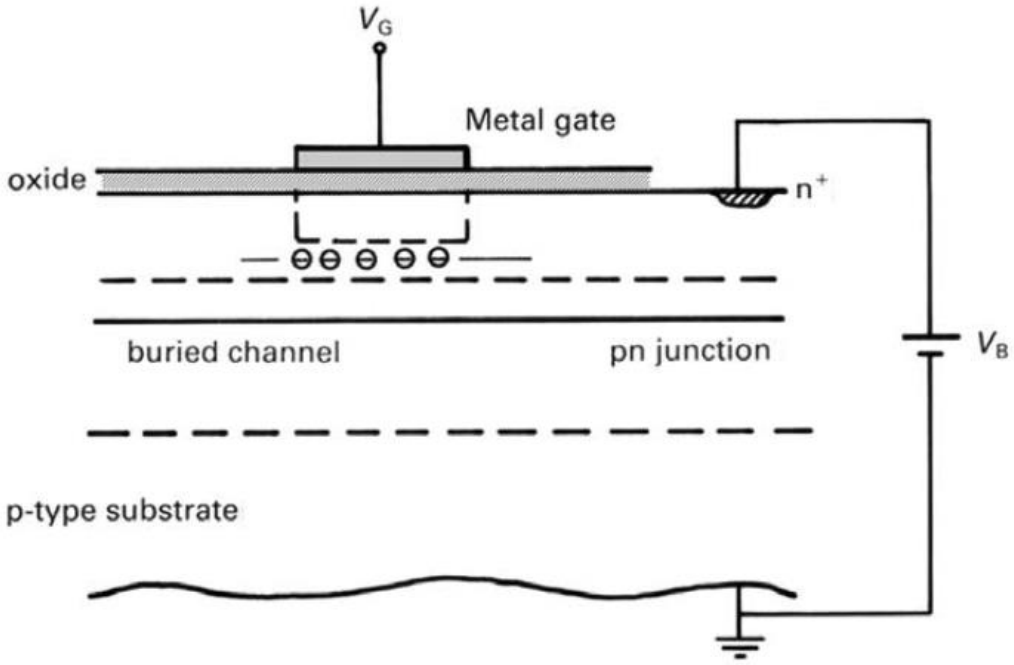
- a pocket of electrons with charge Q is allowed through the final output gate onto an effective storage capacitance C
- causes an instantaneous charge V = Q/C in the voltage of the input line of the on-chip transistor used as a source follower
- , which in turn yields a voltage change at the output line.
- the readout is destructive (it can be read once)



7.3.3 Buried-channel CCDs

- surface-channel CCD
  - The most positive potential liens on the silicon surface immediately under the insulating oxide layer.
  - Electrons are stored and transferred at the surface of the silicon semiconductor.
  - because of many crystal irregularities and defects in the crystal lattice, they can readily “trap” charge.
  - **very poor charge-coupling and severe image smear**

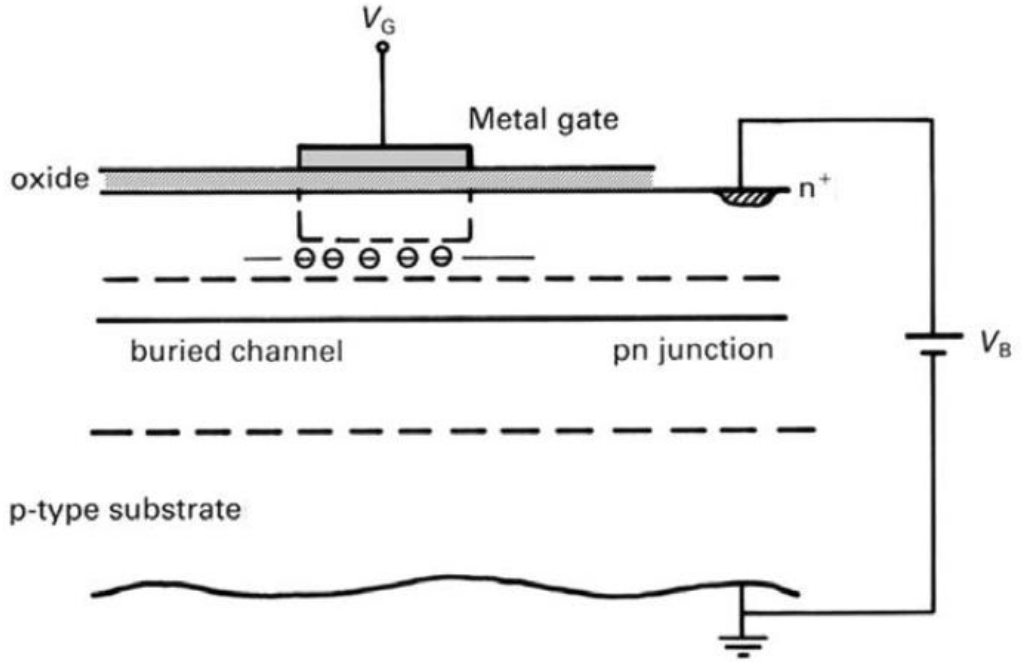
- Buried-channel CCD
  - another layer of silicon is grown onto the existing p-type substrate to separate it from the insulating layer.
  - when adopting n-type layer, a more complex depletion region is created with a potential minimum.

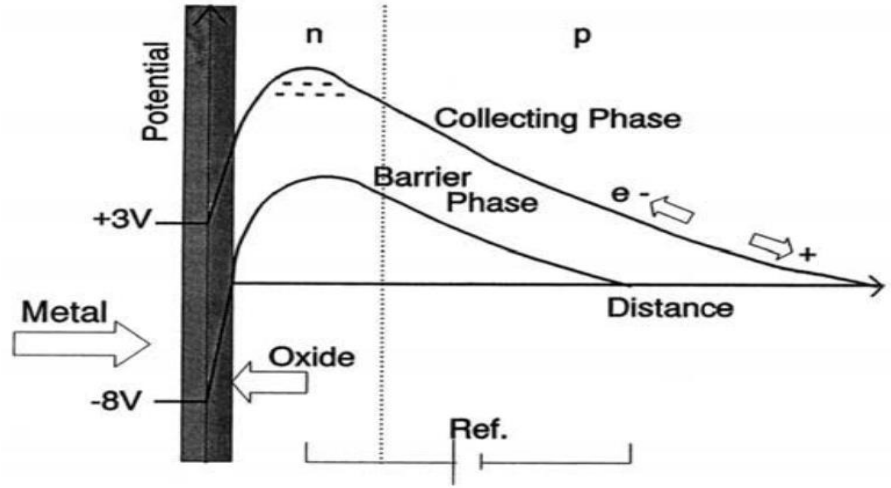


7.3.3 Buried-channel CCDs

- the pn junction
- the most positive potential occurred on the n-side but within the depletion region.
- If a voltage more positive than any of the gate voltages is applied to this n-type layer, a depletion region will form at the pn junction.
- It is important that the n-type region be completely depleted of majority carriers (electrons) in order to **distinguish** electrons created by absorption of photons.
- the applied gate voltage is negative relative to the n-channel potential
  - majority carriers (electrons) are repelled away from the surface in an n-MOS capacitor.

- Charge transfer within the bulk silicon is **very efficient** because the number of trapping sites is considerably fewer and they are much less noisy.





7.3.3 Buried-channel CCDs

$\rho = eN_D$ in the fully depleted n-type

$\rho = -eN_A$ in the p-type layer

t : the depth of the n-type layer

x_n : the location of the potential maximum relative to the pn junction

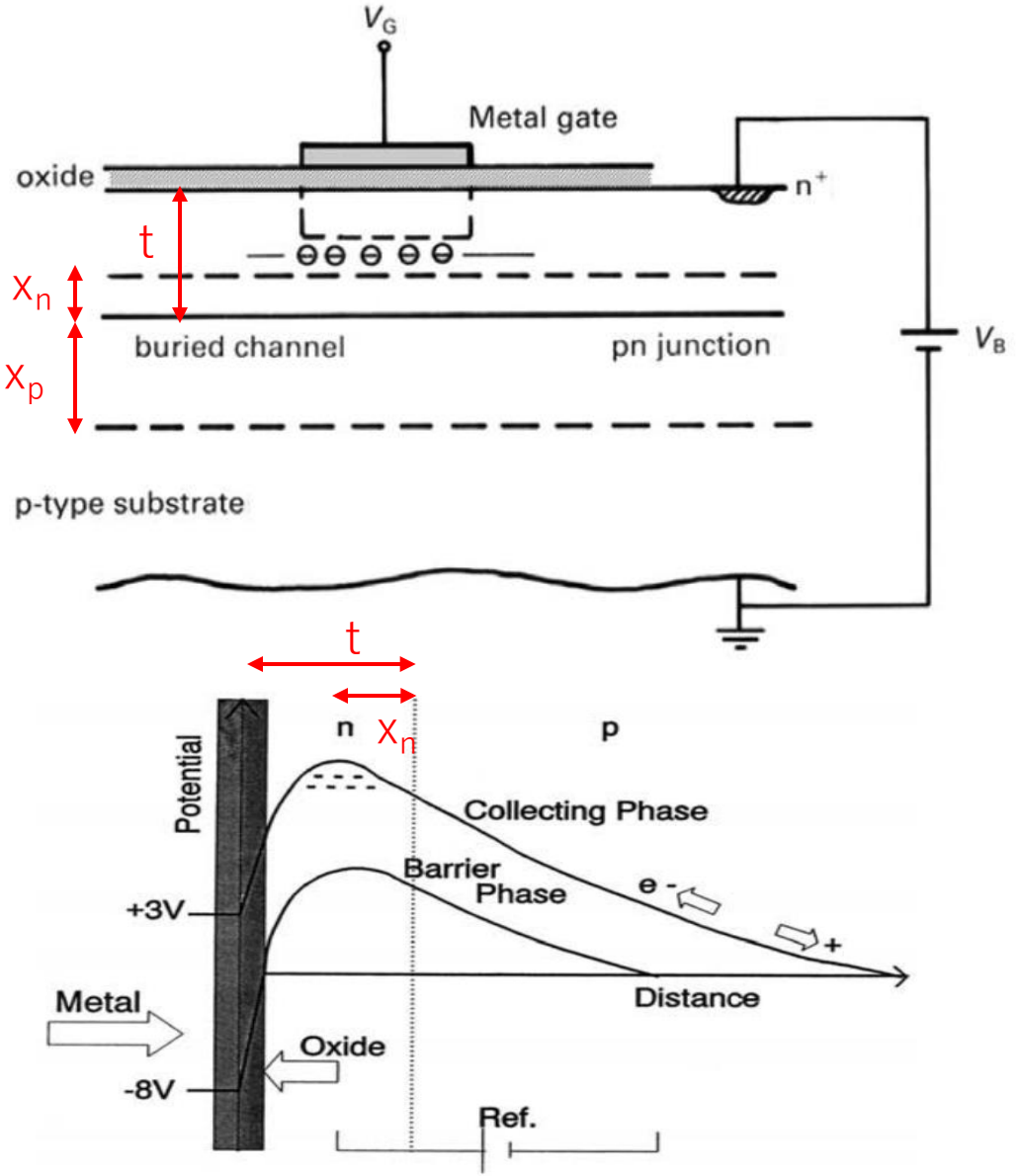
x_p : the depletion depth of the p-type region

$$x_n = t - x_p(N_A/N_D)$$

$$V_2 = V_{max} - \frac{eN_D}{2\epsilon_{si}}(x - x_n)^2$$

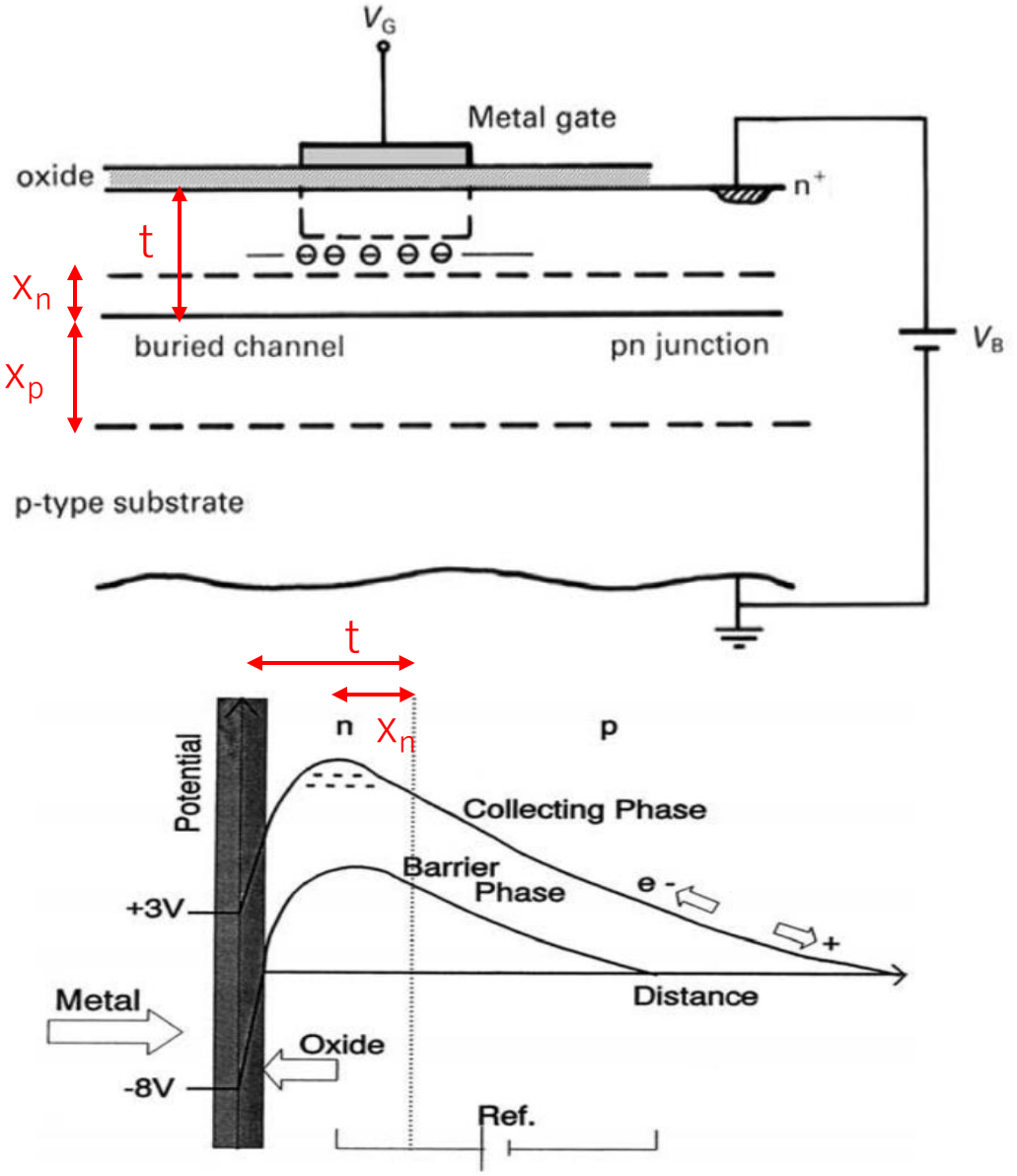
V_2 : the variation of potential in the n-type region from x = 0 to x = t

V_{max}: the channel's maximum potential which is determined by **the junction potential** and **the ratio of acceptor-to-donor concentrations**.



7.3.3 Buried-channel CCDs

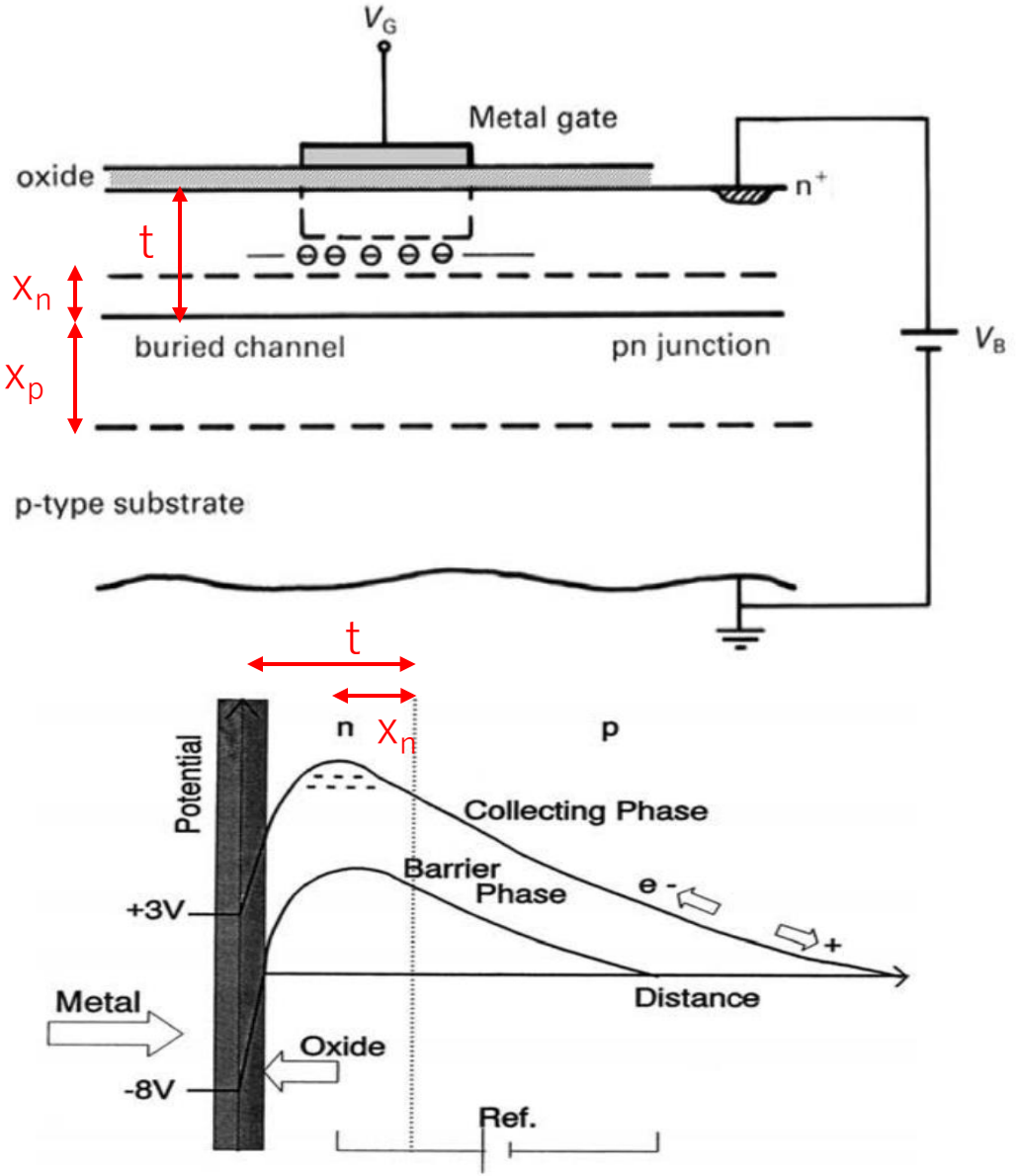
- The effective capacitance per unit area for an empty potential well
  - is the combination of the oxide and depletion capacitance of width t-x_n
  - $C_{eff}^{-1} = \left(\frac{d}{\epsilon_{ox}}\right) + (t - x_n)/\epsilon_{Si}$
- When electrons are generated by photon absorption they will move to the potential maximum and remain there, which causes a portion of the storage well to become un-depleted.
  - $C_{eff}^{-1} = \left(\frac{d}{\epsilon_{ox}}\right) + (t - x_n - (Q/2N_D))/\epsilon_{Si}$
  - Q is the electron surface density
- With typical values for the parameters the full-well capacity is lower than the surface-channel CCD, but charge transfer efficiency is greatly improved.



7.3.3 Buried-channel CCDs

- For high performance
  - electrons are defined in depth (z)
  - electrons are free to move from side to side (x,y-direction)
  - ＞ n-type on p-type substrate

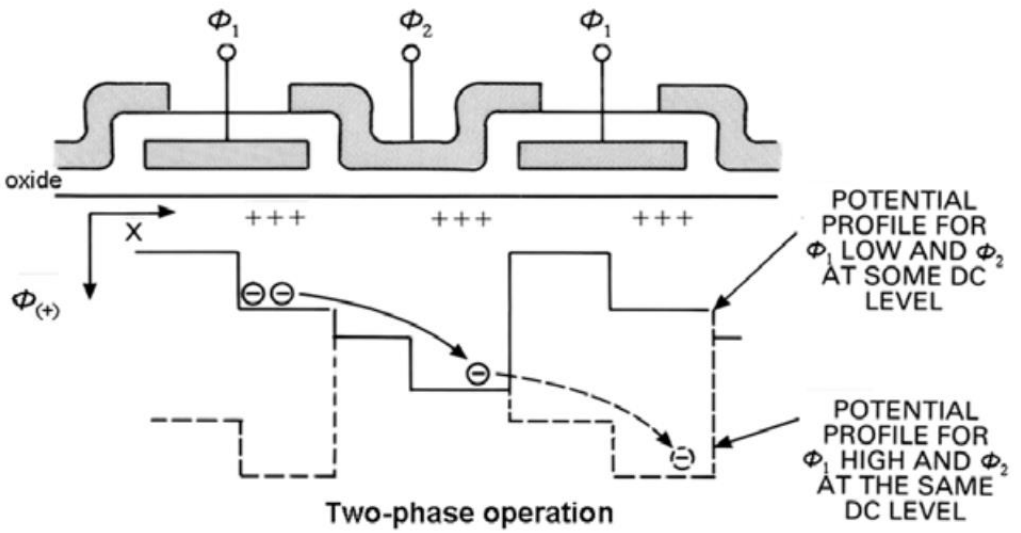
- Narrow columns of heavily doped n-type material are diffused into the normal n-type region
  - produce channel stops in order that electrons are move only in y-direction



7.3.4 Two-phases, four-phases, and virtual-phase CCD

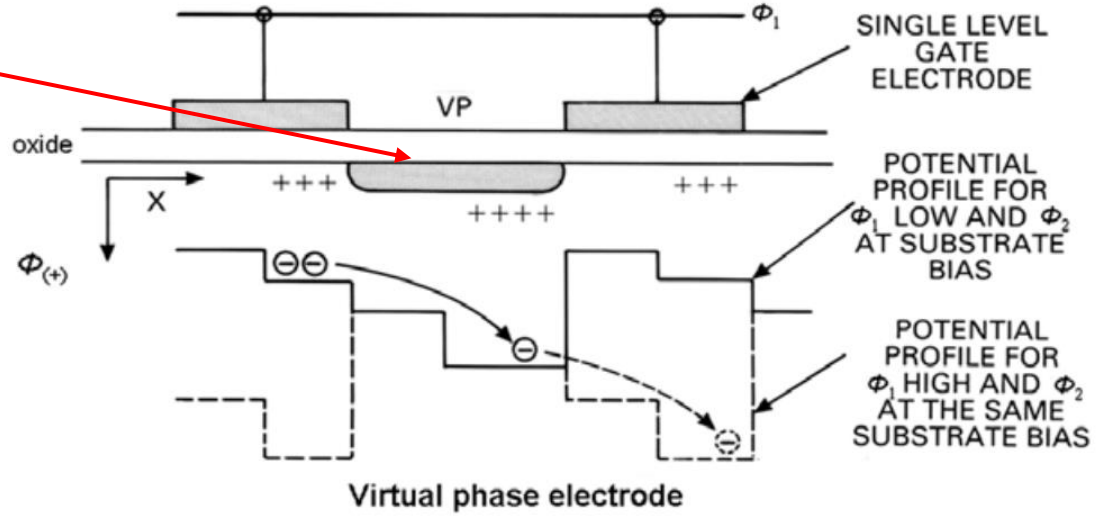
- a two-phase CCD
  - bi-directional charge motion is not required.
  - an “implant” is diffused into one-half of the substrate below each of the two electrodes.
  - this layer affects the depth of the depletion region immediately beneath it in such a way that the depletion is always greater under the implant.

- changing the ϕ_1 and keeping ϕ_2 constant, electrons can be moved left to right.



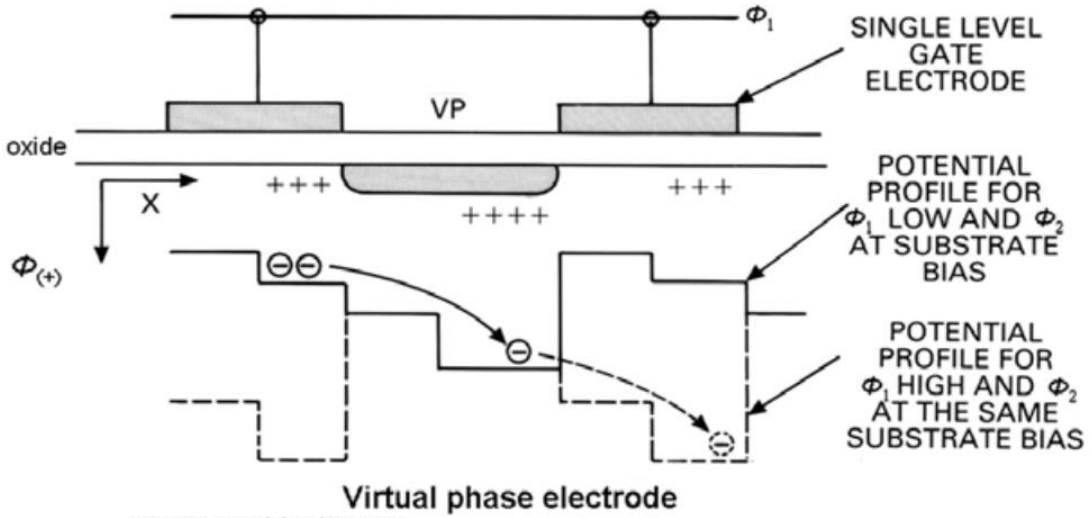
7.3.4 Two-phases, four-phases, and virtual-phase CCD

- “virtual-phase” CCD
  - the first single-clock CCD
  - developed by Texas Instruments Corp.
- One electrode was left at a constant voltage to produce an intermediate depletion region.
- Only one electrode need be physically present and the other half of the pixel is left clear and uncovered except for its implant.
- a series of potential steps created by different levels of surface doping.

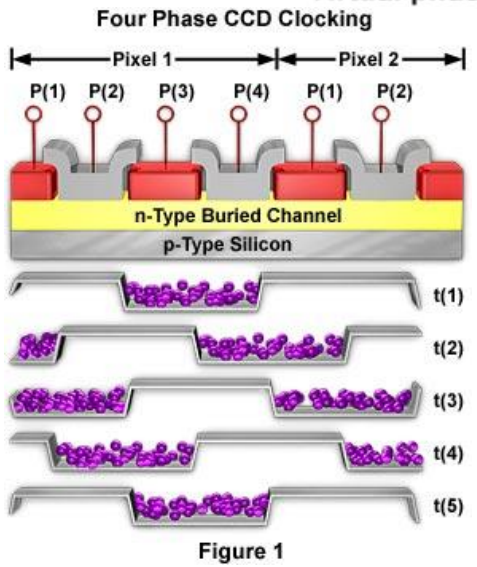


7.3.4 Two-phases, four-phases, and virtual-phase CCD

- Two-phase CCD structure was chosen to permit an improved response to blue light by minimizing the amount of absorption due to the polysilicon (conducting) electrodes when the chip is frontside-illuminated.



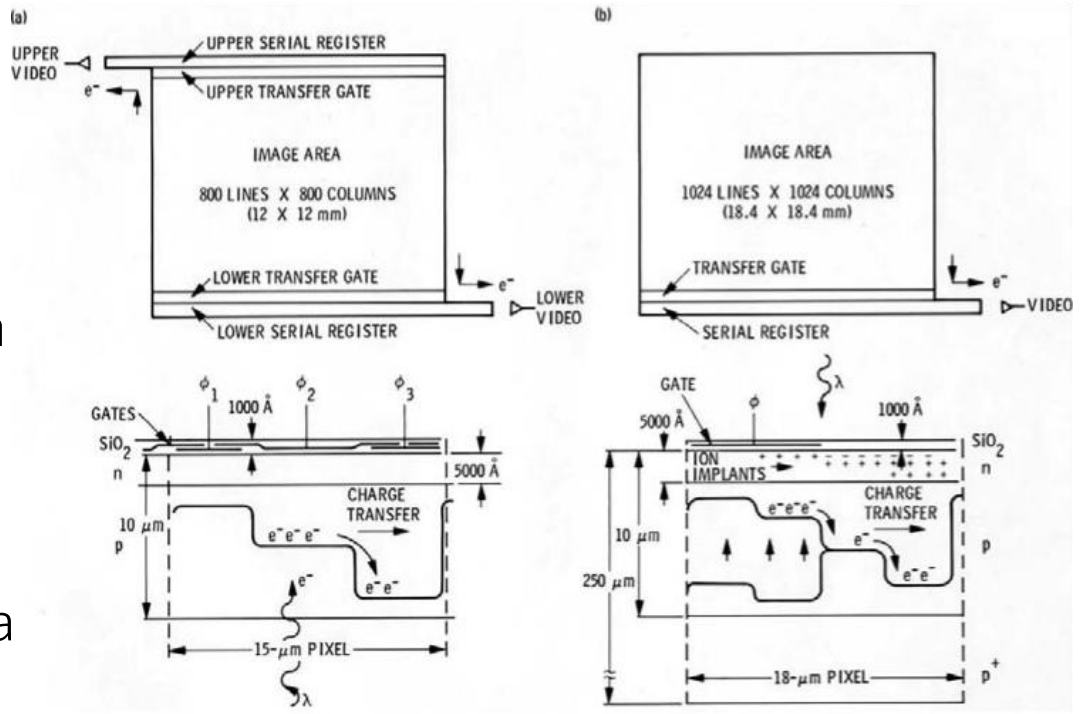
- four-phases CCD
  - complete control over all combinations of phases
  - can be used for special applications involving two alternating image scenes
- the animation of two/three/four CCD model
  - https://www.olympus-lifescience.com/ja/microscope-resource/primer/java/digitalimaging/ccd/shiftregister/



https://www.olympus-lifescience.com/ja/microscope-resource/primer/digitalimaging/concepts/fourphase/

7.3.5 Backside-illuminated CCD

- blue light is easy to absorb in the electrodes.
  - few photons arrive in the depletion region
  - if frontside-illuminated
- the CCD can be turned over and illuminated from the backside!
  - thinned CCD was developed
  - high sensitivity to blue light with short absorption length.
- disadvantage
  - the thinned CCDs are more mechanically fragile a prone to warping.
  - interference “fringing” can occur due to multiple reflections internal to the CCD substrate or between the silicon



7.3.6 Multi-pinned phase CCD

- the dominant contributor to the dark current in CCDs was thermal generation due to surface “states” at the Si-SiO_2 interface.
- surface dark current is 10^2-10^3 greater than dark current generated by the bulk of the CCD
- Two factors control dark current at the silicon-silicon dioxide “interface”
  - the density of interface states
  - the density of free carriers (holes and electrons)
    - in case of CCD, filling the interface state with electrons **maximizes** the dark current from the surface states.

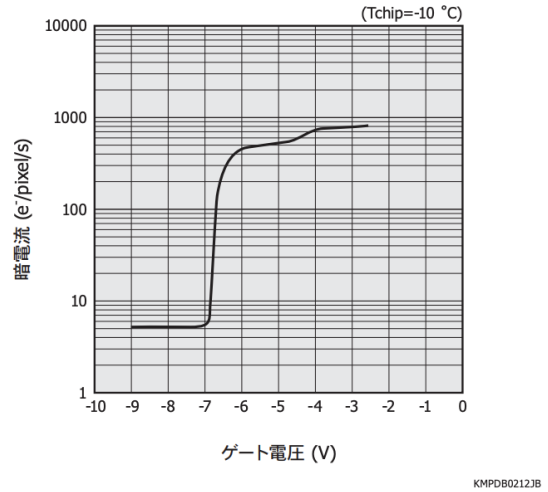
- Dark current is now controlled solely by the density of interface states and is thus dependent on fabrication processes.

7.3.6 Multi-pinned phase CCD

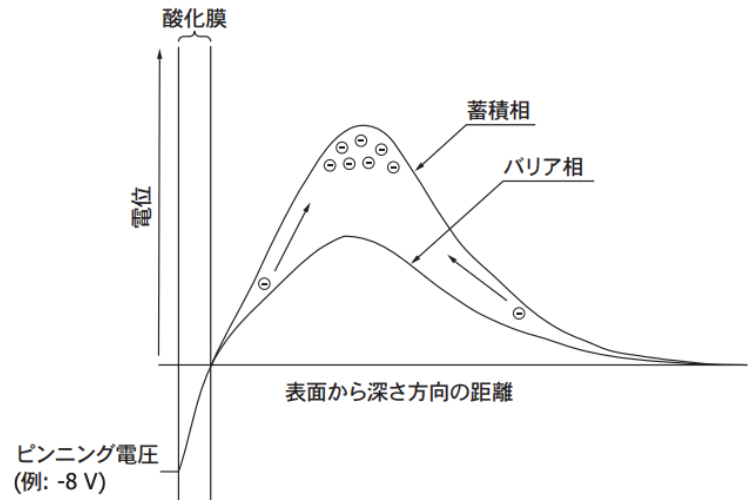
- Multi-Pinned phase (MPP) CCD
  - designed in a special way to allow operation in a totally inverted mode(反転状態)
  - all the gate electrodes are set very negative to the substrate.
  - dark current is reduced.

- To obtain any charge storage capacity while totally inverted the potential of one or more phases **must be offset from the others**.
  - doping the silicon with boron for three-phase MPP CCD

[図2-13] 暗電流–ゲート電圧 (S9974-1007, 代表例)



[図2-12] MPP動作時の電位分布図



https://www.hamamatsu.com/content/dam/hamamatsu-photonics/sites/documents/99_SALES_LIBRARY/ssd/ccd_kmpd9002j.pdf

7.3.6 Multi-pinned phase CCD

- Care must be exercised with CCDs using MPP if the extremely low dark current is required.

- If the CCD becomes saturated, trapped charges will raise the dark current.
- “spurious charge” (偽電荷)
  - produced during each pixel transfer and has a shot noise behavior which can overwhelm the on-chip amplifier noise and dominate the observed readout noise of the chip.
  - for example, 1 electron of spurious charge per 10-pixel transfer, this process would have resulted in 102 electrons and 10e^- rms noise. (3-7 e^- rms for the on-chip amplifier)

- **Three strategies** to overcome shot noise caused by spurious charge production

7.3.6 Multi-pinned phase CCD

- **Three strategies** to overcome shot noise

1. slow down the rise time of the drive clocks
   - by adding an RC network at the output of the clock driver board to allow the holes to return to the channel stops slowly.

2. Limit the clock voltage swing to the smallest value possible consistent with good charge transfer efficiency
   - reduce the driving electric fields and the acceleration of the charges; less spurious charge will be generated

3. a “tri-state” clocking scheme
   - an intermediate clock level is established
   - a slow transition from the inverted level to the intermediate level followed later by the completeswingallowsthetrappedholestobereleasedslowlyfromtheoxide.

7.3.6 Multi-pinned phase CCD

- The vertical registers are inverted to produce low dark current by slowing down the clock edge.
- The horizontal registers of MPP CCD do not receive the MPP implant.
  - the horizontal register is clocked much more rapidly and would produce significant amounts of charge if it was being continuously brought in and out of inversion.

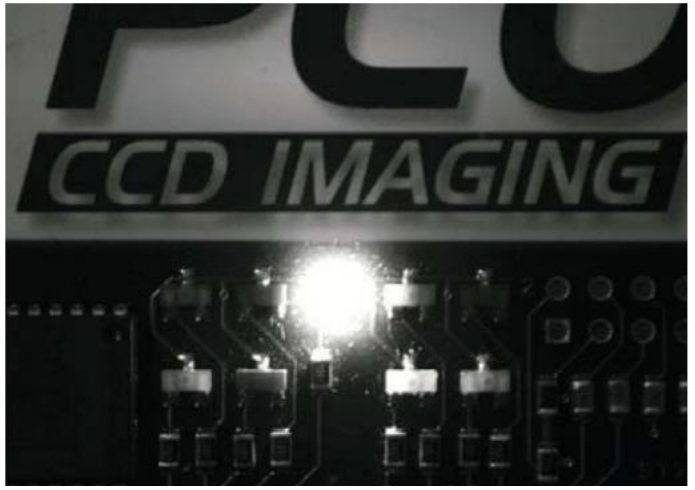
7.3.6 Multi-pinned phase CCD

- “anti-blooming”
  - an advantage other than dark current offered by MPP CCD
  - when there is too much light in a pixel, the well capacity is saturated, letting the exceeded electrons flow into the neighboring pixels. > “blooming”

  - ϕ_3 : inverted all the time
  - phases 1 and 2 are **slowly** switched between the inverted state and just above the optimum full-well voltage

  - This process (MPP) of back-and-forth switching continues during the entire integration period and **inhibits the saturating pixel from blooming** and **bleeding** charge up and down the column.

with blooming



without blooming

https://www.tokyoinst.co.jp/product_file/file/PC03_tec06_ja.pdf