McLean Seminar

Sec 7-7.2.1

7. Charge-coupled devices

・detector : convert electromagnetic energy into an electrical signal

・CCD(charge-coupled device) : dominant

→consider more detail

7.1 THE ERALY YEARS
7.1.1 Invention and development

- charge-coupling principle : invented in 1969
- larger image-forming devices (100 × 100 pixels) : introduced in 1973
  - 2048 × 4096 pixels with no wires or structure on three sides
    →now available
  - most observatories using CCD “mosaics”
    composed of many “close-butted” devices

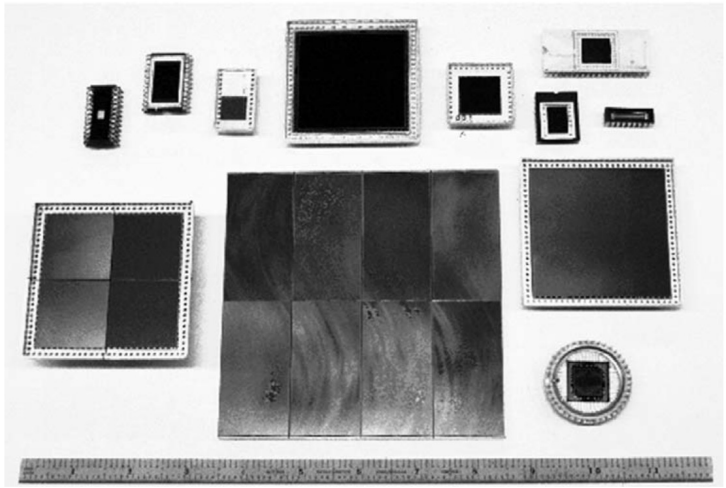


Figure 7.1. A collection of CCDs including eight large-format (2 K × 4 K) devices butted together to form a 64-megapixel mosaic. Credit: Gerry Luppino.

7.1.2 The astronomical push

・recognition the potential of CCDs in the early 1970s

→ initiate a program for the development of large-area CCD imagers for Galileo mission to Jupiter in 1973 (JPL, NASA, TI Incorporated)

→Galileo spacecraft was launched in 1989 and success

・1973~1979 : TI developed CCD arrays of 100×160 pixels, 400×400 pixels, 500×500 pixels, 800×800 pixels array

・testing and evaluation at JPL

・1974 : image of the Moon by 20.3cm telescope with 100×100 Fairchild CCD

・1976 : first astronomical imagery with CCD on a professional telescope (61-inch telescope on Mt. Pigelow (Arizona))

・ CCD images of Jupiter and Saturn using a special filter to pick out methane gas

・at the same time, NASA made contracts for the procurement of instruments for Space Telescope

・proposal for the inclusion of CCD cameras(low noise) on the Space Telescope was accepted

7.1.2 The astronomical push

・Electro-optics Division of RCA (Radio Corporation of America) was working on CCDs
→began testing these devices in the late 1970s
・First, John Geary (Harvard) tried an unthinned devise on the 1.5m and 60cm telescopes on Mt. Hopkins
→splendid result
・very first thinned backside-illuminated CCD was put on the telescope on Mt. Hopkins
→remained for a decade
・TI chips evolved through a program of systematic development toward the goal of 800×800 array
・major constraint : able to survive harsh radiation environment around Jupiter
・”buried-channel” and “virtual-phase” CCD evolved
・75,000 CCDs were manufactured

7.1.2 The astronomical push

・other companies were also beginning to develop CCDs (1974~1977)

・Fairchild Semiconductor produced 100×100 CCD in 1974

・Kitt Peak National Observatory (KPNO) began a program of development of CCDs

・Fairchild CCD201 and CCD202 image sensors (designed for TV applications) were capable of high performance

↔serious impediment for astronomical work due to the interline transfer construction

・columns of picture elements were alternately light-sensitive and insensitive

→devices were half blind

7.1.2 The astronomical push

・late 1970s : great frustration about the lack of access to CCD technology by the mainstream astronomical community

・development of Wide-Field/Planetary Camera(WFPC)

・many people were aware of the sensitivity and the scientific potential of CCDs

・little commercially available products

→other forms of less suitable solid-state imagers were tried

→appearance of 512×320 RCA CCDs in the late 1970s made relieve

・first RCA CCDs : frontside-illuminated, poor response to blue light

⇔soon, the thinned backside-illuminated CCDs appeared

・outstanding sensitivity over a huge spectral range better than TI chips

・weakness : 5-10 times noisier than the TI CCD

→later RCA CCDs were much better

7.1.2 The astronomical push

- early 1980 : unexpected source of astronomical CCDs appeared
  - Craig Mackay (Cambridge) : had been working on silicon vidicons
    - silicon vidicon : good spectral response, but noisy

      →need a very low noise amplifier design

      →work with GEC Hirst Research Centre designing metal oxide semiconductor (MOS) transistors (easily available)
      - GEC : had a very advanced CCD program
        - GEC CCDs : typically reported as 7 electrons
    - Craig designed a CCD drive system based on an existing vidicon

7.1.2 The astronomical push

・1981 : the number of independent astronomy groups CCD systems had grown from 5 to 20
  ・devices in use are only from TI, RCA, and GEC
    ・GEC : low-noise
    ・RCA : high quantum efficiency
    ・TI : should have both properties↔problems with blue sensitivity and not available for sale

⇨detailed studies of the TI chips→advanced the understanding of CCDs and their optimization

・1985 : most exciting prospect
  ・Tektronix Inc. produce scientific grade CCDs with large formats and outstanding performance
    ・initial goal : 512×512 array with good-sized pixels(0.027mm)
    ・final goal : 2,048×2,048 pixels

    ↔large numbers of defects (“pockets”) due to fabrication or processing problem
      →devices became unusable
        ・collaborate with other parties and followed every effort
          →began to ship CCDs to customers (1988)
    ・CCD group was separated into Silicon Imaging Technologies, Inc. and supplied CCDs for SDSS

7.1.2 The astronomical push

・the time of dry spell in CCD supplies

・Richard Aikens (founder of Photometrics Ltd.) contracted “silicon foundry” to produce a custom CCD with 516×516 pixels

→outstanding success

・early 1990s

・Dick Bredhauer and his team at Ford Aerospace made a 4,000×4,000 CCD with 15um pixels

・Photometrics coted chemical phosphor (Metachrome Ⅱ) which can be applied safely to CCD by vacuum sublimation

→improve the response to blue light

・1988

・Lloyd Robinson constructed a large CCD suitable for spectroscopic applications (400×1,200)

・EEV in UK began a thinning program and a mosaic construction program

・Thomson-CSF in France

・developed a “buttable” version of their excellent low-noise front-illuminated device

7.1.2 The astronomical push

・these approaches : a trend that has continued until now

　・now, astronomers work directly with a silicon foundry and obtain customized CCDs

・Most astronomical developments : concentrate on forming mosaics of high yield formats, and optimizing the response at both ling and short wavelength

7.2 BASIC PRINCIPLES OF CCDs
7.2.1 Charge storage

・CCD : array of individual picture elements (pixels)

・pixel : absorb photons and utilize the energy to release an electron within the semiconductor

・when making an imaging device

・don't want photon-generated electrons to move from the site where the original photons impact

・special electrostatic field are required to confine the electron within a pixel

・next photon

・need to create a storage region capable of holding many charges

→apply metal electrodes to the semiconductor silicon together with a thin (100nm) separation layer (silicon dioxide(electrical insulator))

→like a parallel-plate capacitor and store electrical charge

= MOS (metal oxide semiconductor) structure

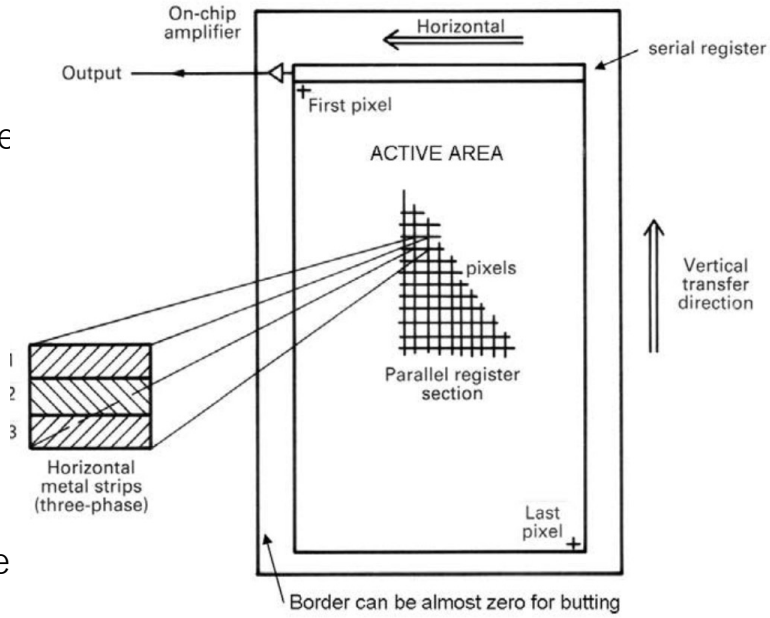


Figure 7.3. The general layout of a CCD as a grid of pixels on a slab of silicon.

7.2.1 Charge storage

・MOS

・apply voltage to the metal electrode→electric field is generated inside the silicon slab

・when the material is p-type (usual case, holes are majority carriers)

・positive voltage on the metal gate

→repel the holes which are in the majority and generate a depletion region of charge carriers

・absorb a photon in this region

→produce an electron-hole pair

→hole : driven out of the depletion region

electron : attracted towards the positively charged electrode

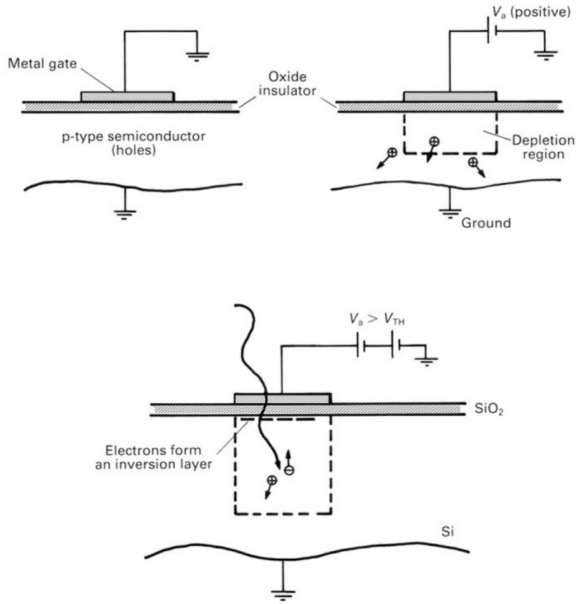


Figure 7.4. The development of a single metal oxide semiconductor (MOS) storage well, the basic element in a CCD, for different applied gate voltages.

7.2.1 Charge storage

・MOS capacitor : combination of two parallel-plate capacitors (oxide capacitor + silicon depletion region capacitor)

⇨capacitance

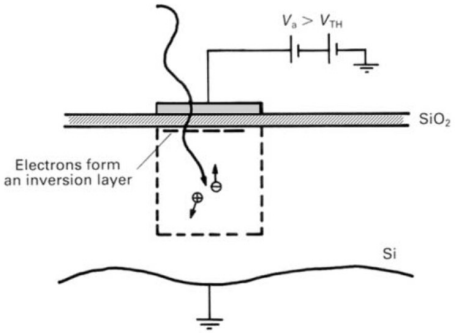
proportional to the area of the plates (electrodes)

inversely proportional to their separation

・control the voltage on the plate

→change the depletion width, control the capacity to store charge

・depletion region : electrostatic “potential well” or “bucket” and collect many photo-generated charges



・number of electrons stored $Q = CV/e$

e:charge on the electron $1.6\times10^{-19}C$, V:effective voltage,

C:capacitance $C = A\kappa\varepsilon_0/d$(parallel-plate formula, A:area of the pixel or gate electrode, d:thickness of the region, κ:dielectric constant of the SiO_2 insulator, ε_0:permittivity of free space 8.85×10^{-12} farad/m)

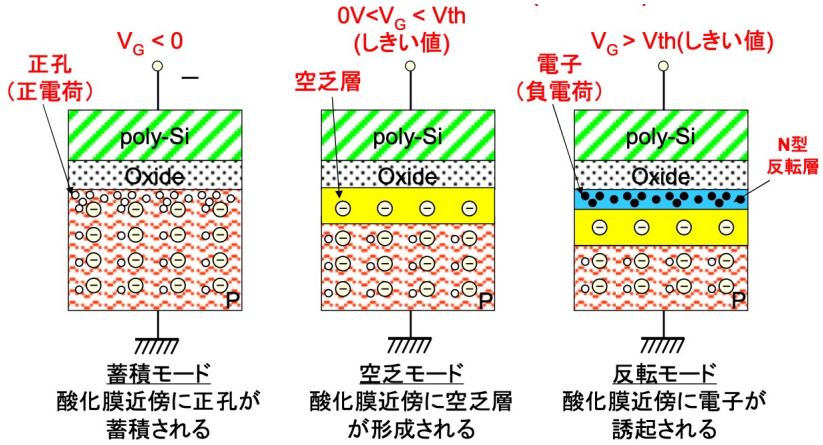
・voltage on the electrode increases → depth of the well increases

・other ways are needed to create sidewalls of the wall

・eventually, at a “threshold” voltage, the minority charge carriers (electrons for a p-type semiconductor) will be attracted to the electrode

→form an inversion layer

7.2.1 Charge storage



・p-MOS capacitor's composition

・p-type (boron-doped) Silicon

・100nm thick thermally grown layer of $\mathrm{SiO_2}$ (like a dielectric insulator)

・conductive (metallic) gate made of deposited polysilicon (silicon with randomly oriented crystal grains)

・apply a negative voltage to the gate when the silicon substrate is at ground potential

→highly conductive layer of holes accumulate at the $\mathrm{Si-SiO_2}$ interface in a few nanoseconds

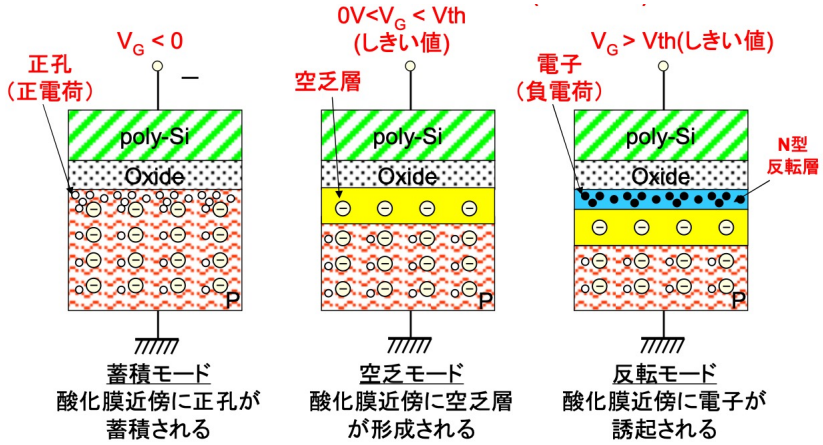
＝accumulation mode

・capacity per unit area of the oxide : $C_{OX} = \frac{\varepsilon_{OX}}{d}\ (\mathrm{F/m^2})$

d:thickness of the oxide insulator, $\varepsilon_{OX} = \kappa\varepsilon_0$:permittivity of $\mathrm{SiO_2}$ $3.45\times10^{-11}\ \mathrm{F/m}$

・when there are two insulating layers ($\mathrm{SiO_2}$, silicon nitride ($\varepsilon_{nit} = 6.63\times10^{-11}\ \mathrm{F/m}$)) capacities add in series⇨ $C_T = C_{OX}C_{nit}/(C_{OX} + C_{nit})$

7.2.1 Charge storage



・apply positive voltage to the gate

→holes are driven away from surface, and negatively charged boron ions are left

→create a depletion region with no mobile charge carriers

・the number of holes driven away in depletion mode = the number of positive charges on the gate electrode

$Q_i = eN_A x_d$

Q_i $(\mathrm{C/m^2})$:ionized acceptor charge concentration under the depleted gate

x_d (m):depth of the depletion region

N_A $(\mathrm{atoms/m^3})$:concentration of boron (acceptors)

e:numerical value of the charge on the electrons

・depletion region is non-conductive⇨acts like an insulator

capacitance $C_{\mathrm{dep}} = \varepsilon_{\mathrm{Si}}/x_d$ ($\varepsilon_{\mathrm{Si}} = 1.04\times10^{-10}$ F/m, dielectric constant~11.7)

⇨gate capacitance in depletion mode is the series combination

7.2.1 Charge storage

・gate voltage : constant throughout its thickness (conductor)
  ・voltage drop across the oxide layer
    →voltage in the depleted p-type silicon depend on the charge distribution
    →eventually drop to the ground potential of the substrate
    ・variation of voltage(V), depth(x), Poisson's equation
      →$\frac{d^2V}{dx^2} = -\frac{\rho}{\varepsilon_{Si}}$　ρ:charge density, origin(x=0) is $\mathrm{Si-SiO_2}$ interface
      principle: $\rho = e[p + n + N_A + N_D]$
      p:number density of free holes, n:number of free electrons,
      $N_A(\mathrm{atoms/m^3})$:number density of localized fixed ionized acceptors,
      $N_D(\mathrm{atoms/m^3})$: number density of fixed ionized donors
      ・electric field sweep away most free carriers in the depletion region
      ⇨ $\rho = -eN_A$ (p-channel)　(absence of holes⇨sign is negative)
      ⇨ $\frac{d^2V}{dx^2} = \frac{eN_A}{\varepsilon_{Si}}$

7.2.1 Charge storage

・$\frac{dV}{dx} = 0,\ V = 0(x = x_d)$

→$V = \frac{eN_A}{2\varepsilon_{Si}}(x - x_d)^2$

→most positive voltage occurs at $\mathrm{Si} - \mathrm{SiO_2}$ interface (x=0)

surface voltage: $V_s = \frac{eN_A}{2\varepsilon_{Si}}x_d^2$, surface electric field: $E_s = \frac{eN_A}{\varepsilon_{Si}}x_d$

・electric field: 0(metallic gate), V_{OX}/d(oxide), decrease linearly to 0(depletion region)

・potential: constant(gate), drop by $V_{OX} = E_s d$(oxide layer), decay quadratically from V_S to 0

7.2.1 Charge storage

・MOS capacitor in depletion mode: basic element of a surface channel CCD

gate voltage $V_G = V_{OX} + V_S = E_S d + V_S = \frac{eN_A x_d}{\varepsilon_{Si}} d + \frac{eN_A}{2\varepsilon_{Si}} x_d^2$

・photon-generated electrons collect at the surface

→number of ionized acceptor atoms decreases

→depletion region becomes smaller

・for fixed V_G, effective voltage drop V_Q at the gate

$V_Q = V_G - \left(\frac{eN_e}{C_{OX}}\right)$ N_e:signal charge measured in electrons

7.2.1 Charge storage

・charge storage capacity of the MOS capacity

= amount of charge required to bring the surface potential back to 0V

・gate and substrate potentials are fixed

→signal electrons at $\mathrm{Si}-\mathrm{SiO_2}$ interface are shared between oxide and depletion capacitances

→capacitors are parallel

・change of surface potential(V_S)

$\Delta V_S = -Q/(C_{\mathrm{OX}} + C_{\mathrm{dep}})$　Q:charge

・ C_{OX} dominates

→ $Q \sim C_{\mathrm{OX}} \Delta V_S$

→full-well capacity $N_{\mathrm{FW}} = C_{\mathrm{OX}} V_S / e$

→there are disadvantages to collecting charge at $\mathrm{Si}-\mathrm{SiO_2}$ interface and modified design is needed