McLean seminar

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8.3 Cosmic rays and luminescence

8.4 Bad pixels and charge transfer efficiency

8.5 Noise sources

8.6 Signal processing and digitization

8.3 COSMIC RAYS AND LUMINESCENCE

8.3 COSMIC RAYS AND LUMINESCENCE

- cooled CCD: possible to endure very long exposure time with lower dark current
- High-energy particles (e.g. protons) enter Earth's atmosphere from space and generate secondary particles called muons.
- Muons can be stopped by a thick silicon layer, and released energy can generate around 80 electrons per pixel per micron of silicon.

→ collection depth of 20 mm = a few thousand electrons

→ a muon event can be seen as a bright spot on a CCD image

- Thin CCDs, like backside-illuminated or epitaxial ones, are less affected by cosmic rays than thicker CCDs. High-altitude observatories experience more cosmic ray hits than labs at sea level.

8.3 COSMIC RAYS AND LUMINESCENCE

- Space CCDs face severe issues due to a high number of ionizing particles.
- Galileo (Jupiter probe) CCD camera: Without neutron testing, it would have reached Jupiter with large dark spikes across the array.

→ solution: operated at -120°C instead of the planned -40°C.

- Cassini (Saturn probe) and Hubble CCDs: Operated at -90°C to reduce damage from proton impacts.
- Chandra X-ray Observatory CCDs: Suffered proton-related radiation damage soon after launch, degrading charge transfer efficiency.

8.3 COSMIC RAYS AND LUMINESCENCE

Two major types of damage:

- Ionization damage:

- Caused by electron-hole pairs forming in the gate dielectric (e.g., SiO_2) due to radiation.

- Trapped holes shift the voltage in the clock and amplifier bias.

- Radiation at the Si-SiO_2 interface can break weak bonds, creating interface states, increasing dark current.

- Bulk damage:

- Energetic particles collide with silicon atoms, displacing them from the crystal lattice.

- This causes: Permanent degradation of charge transfer efficiency. Increased dark current and dark-current spikes. Effects on the output amplifier.

8.3 COSMIC RAYS AND LUMINESCENCE

- Cosmic-ray events in ground-based cameras are usually easy to remove from images since they are noticeable and concentrated on a few pixels.

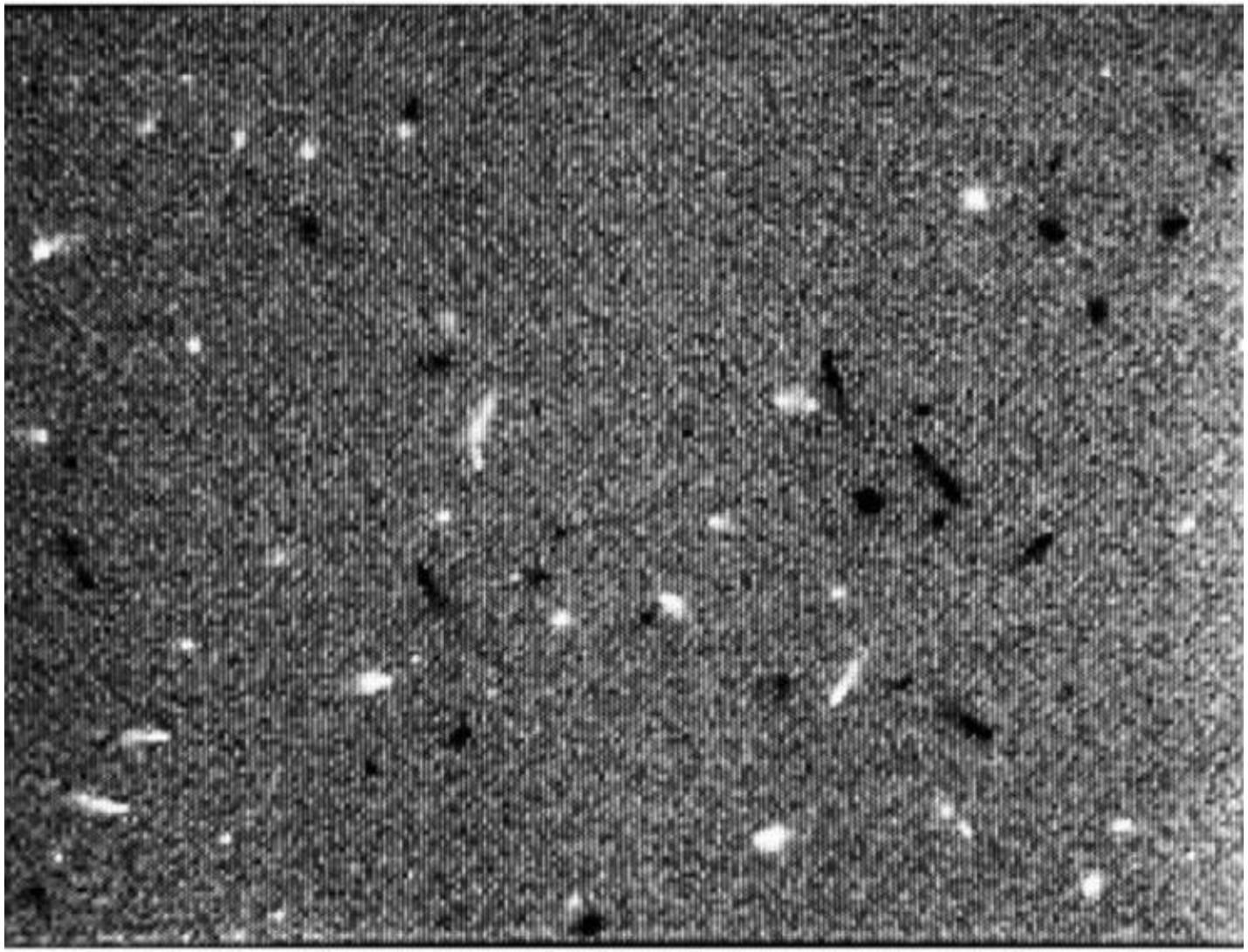
- Removing cosmic rays from non-crowded fields and non-extended objects is straightforward, or by comparing multiple images of the same region since it's unlikely for a cosmic-ray event to hit the same pixel twice in quick succession.

- Early experiments by Craig Mackay from the Institute of Astronomy in Cambridge revealed that cosmic-ray events were a mix of cosmic rays and low-level X-ray emissions from UV and blue-transmitting glass, like Schott UBK7 and GG385.

- X-ray emissions were the dominant cause of the bright spots, not just cosmic rays, which explained why the predicted muon event rate was lower than observed.

- With fused silica windows, the actual event rate was about 1.5–2 events/cm²/min, or 90–120 events per CCD frame per hour of exposure.

difference between two long exposures, where cosmic-ray hits in the second frame appear as dark spots, ionizing particles or high-energy photons.



8.3 COSMIC RAYS AND LUMINESCENCE

Another issue in CCDs and similar devices like infrared imagers is luminescence or glow. This occurs when low-resistance electrical paths act like LEDs, often due to partial shorts between electrodes in the registers.

Incorrect voltages applied to the device, particularly the output transistor amplifier, can also cause this glow.

This effect limits exposure time, but can be controlled by active electronic control or device selection. One approach is to electronically switch off the output transistor during integration to reduce glow.

8.4 Bad pixels and charge transfer efficiency

8.4 Bad pixels and charge transfer efficiency

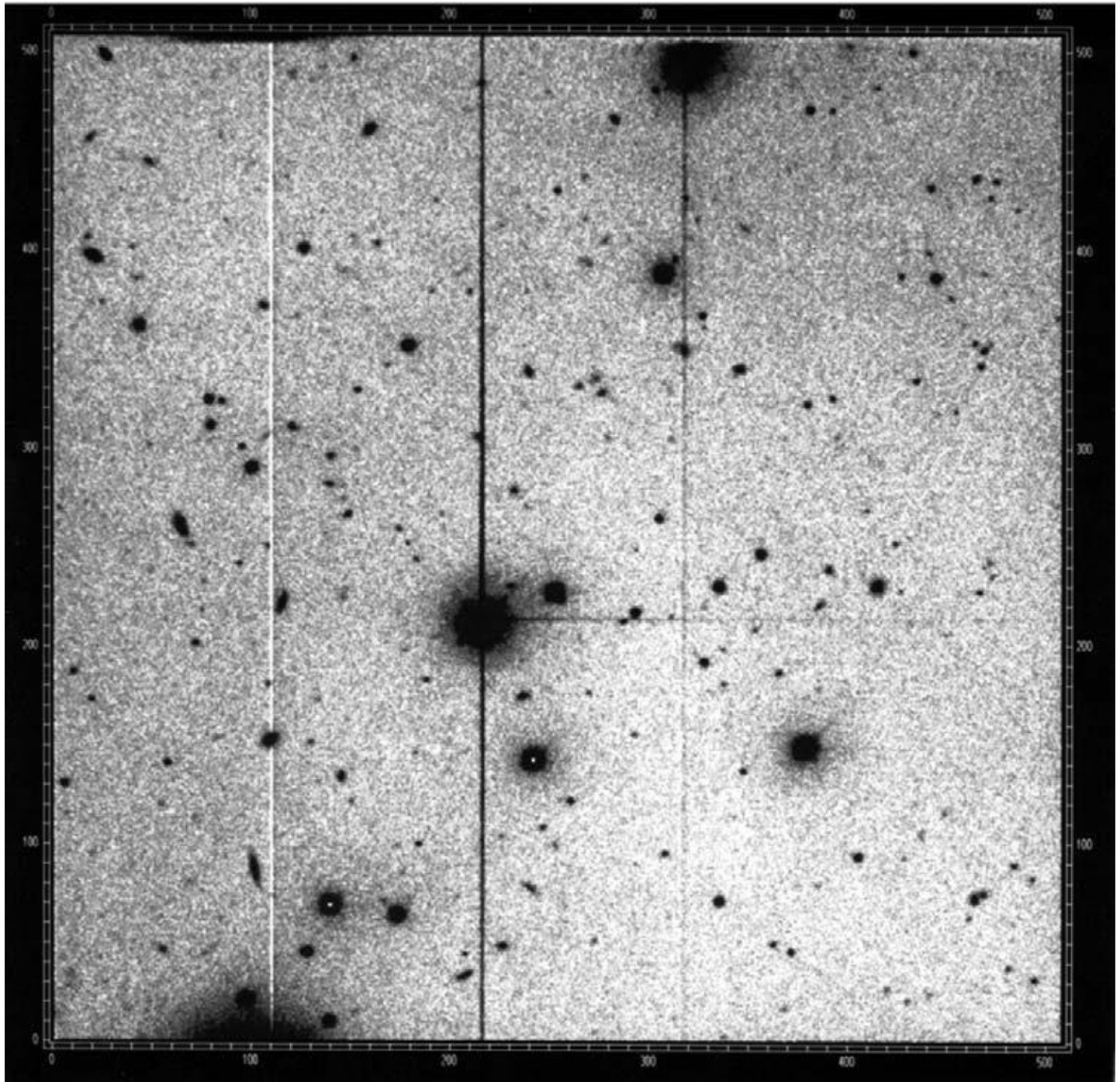
- During exposure, charges accumulate under CCD electrodes and are then moved pixel by pixel through applied clock voltages after the exposure ends.
- the inventors of CCDs (Bill Boyle and George Smith) recognized several issues that could impede the charge transfer process. Problems occur when

- wells are (a) virtually empty, (b) almost full, (c) or when a defective pixel interrupts
- As the wells fill up, the stored charge can distort the electric potential of the applied clock voltage, degrading charge transfer efficiency. When wells are fully saturated, the charges spill over into adjacent pixels in the same column, leading to a vertical spread of charge.

- If the source of light causing saturation is very strong, the adjacent pixels may fill up

→ a streak appears up and down the column = "charge bleeding"

Example of
"charge bleeding"



8.4 Bad pixels and charge transfer efficiency

- Charge Transfer Efficiency (CTE) drops when a fixed amount of charge is "trapped" during each pixel transfer.

→ causes tails to appear on point-like images, aligned with the transfer direction.

- Trapped charge is usually not lost but more often it is "skimmed" to be released later, causing a phenomenon known as "deferred charge".

- Origins of "deferred charge":

- Spurious potential pockets.

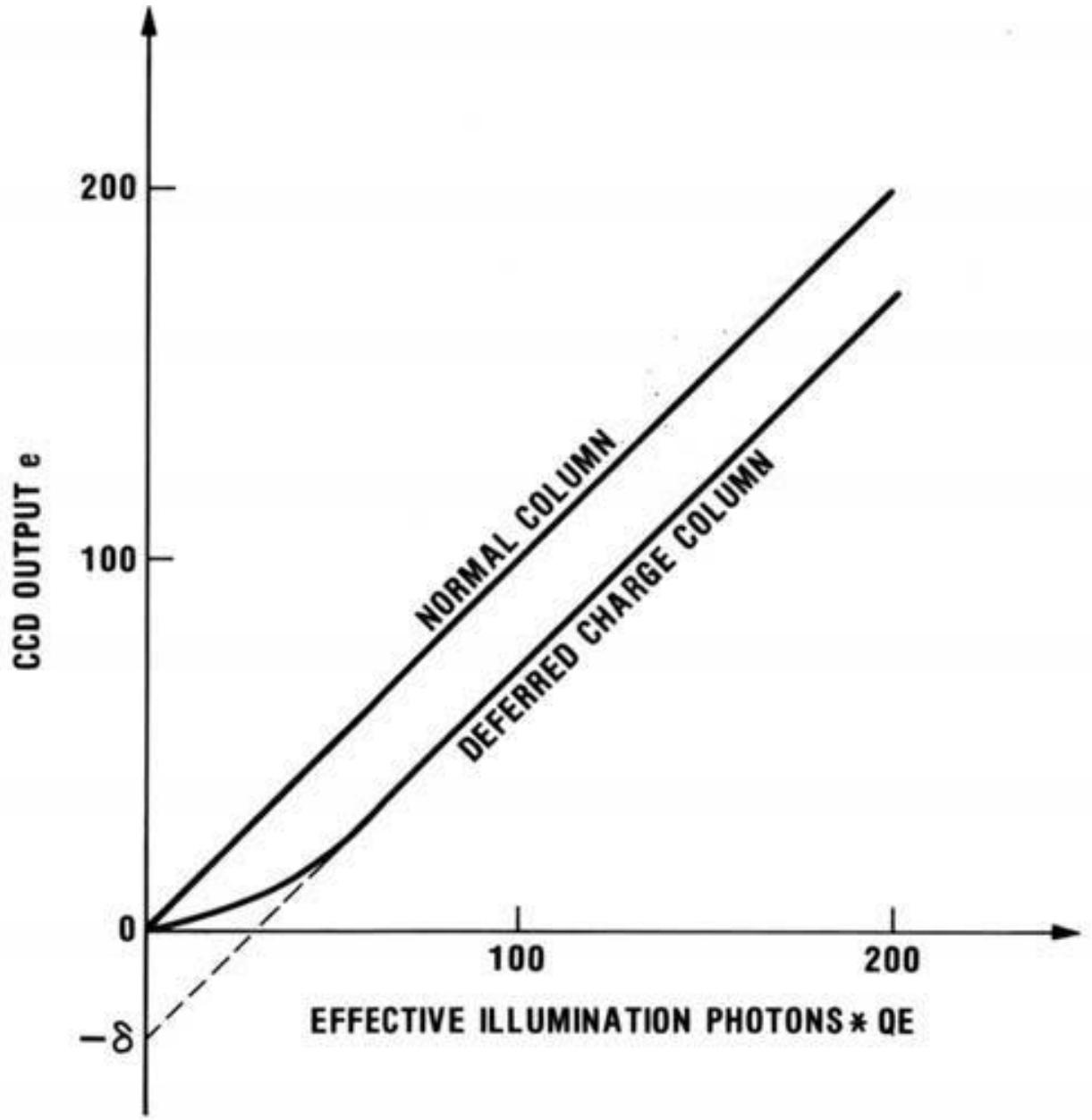
- Design faults leading to specific potential pockets.

- Charge traps associated with impurities.

Number of electrons
at the output of a CCD
v.s. in the original pixel

No trapped charge
→ should follow normal column

Otherwise
→ readout has been deffered



8.4 Bad pixels and charge transfer efficiency

- Poor charge transfer efficiency becomes a concern when there are fewer than ~10 electrons/pixel.

→ concern only in very short exposures, or in spectroscopic applications, where the dispersed background level is below 100 electrons.

- Solution to deferred charge:

"pre-flashing" the CCD with light from an LED is used before each exposure. This adds a small constant charge (called a pedestal) to each pixel, raising the charge level above 100 electrons to improve transfer efficiency.

Note: $\sqrt{100} = 10$ noise electrons added as a penalty

- A large charge pedestal is humorously called a "fat zero". A smaller pedestal to offset deferred charge is called a "skinny zero".

- The common term in astronomy is pre-flash.

8.4 Bad pixels and charge transfer efficiency

Other difficulties related to specific CCD faults:

- Blocked column: A break in one of the polysilicon electrode strips (due to a manufacturing fault) can stop or delay charge transfer in that column.

- Crystal defects: Defects in the silicon substrate can spread into the depletion region during manufacturing, disrupting the semiconductor's properties. These defects act like sponges, absorbing charges and releasing them with delays ranging from milliseconds to hours. Such columns are often irreparable through image processing.

- A charge trap near the beginning of the horizontal (serial) register a disaster as it affects the entire readout process.

- The design of the overlapping electrode structure can create resistance pockets in the channel potential, which trap charges.
- Trapping sites are particularly serious for surface-channel CCDs. Traps would behave like small potholes in the water-in-a-well analogy. These traps fill easily but do not release charges efficiently when the well's floor is raised and lowered.
- The "yield" (歩留まり) of commercial buried-channel CCDs free from all these problems is high.

8.4 Bad pixels and charge transfer efficiency

CTE (Charge Transfer Efficiency) is expressed as 0.99999 per transfer or, in jargon "five nines of CTE", means

- After one transfer, 99.999% of the original charge is successfully transferred.

- After two transfers, 99.998% (0.99999^2) of the original charge remains.

- After 1,000 transfers, 99.00% (0.99999^1000) of the original charge reaches its destination, with 1% spread over the intermediate pixels. Practically, most of that 1% loss is found in the adjacent pixel.

- CTE is a function of temperature, clock frequency("readout rate"), the rise-and-fall times and overlap, and the degree of overlap.
- CTE in the column (parallel) direction differs from that in the horizontal (serial) direction. There can be large variations from one column to another.

8.4 Bad pixels and charge transfer efficiency

- Measuring CTE is not simple
- Qualitatively and quantitively useful method:

overscanning or extended pixel edge response (EPER)

- flood the CCD with light, read out, but "overscan" both axes to generate an image several pixels larger than the actual CCD
- Most CCD controllers permit overscanning, but some CCDs have extra pixels in the serial register, which can confuse the results of overscanning.
- Transfer problems leading to deferred charge can be understood by comparing the signals in imaginary pixels with the dark level and with the illumination level.
- Some investigators calculate an average CTE for all rows or columns, but careful analysis of the overscanned image reveals variations from column to column.

→Averaging may be required to reduce readout noise effects

8.4 Bad pixels and charge transfer efficiency

Formula of CTE:

$$CTE(e^-) = 1 - \frac{Q_d}{NQ_0}$$

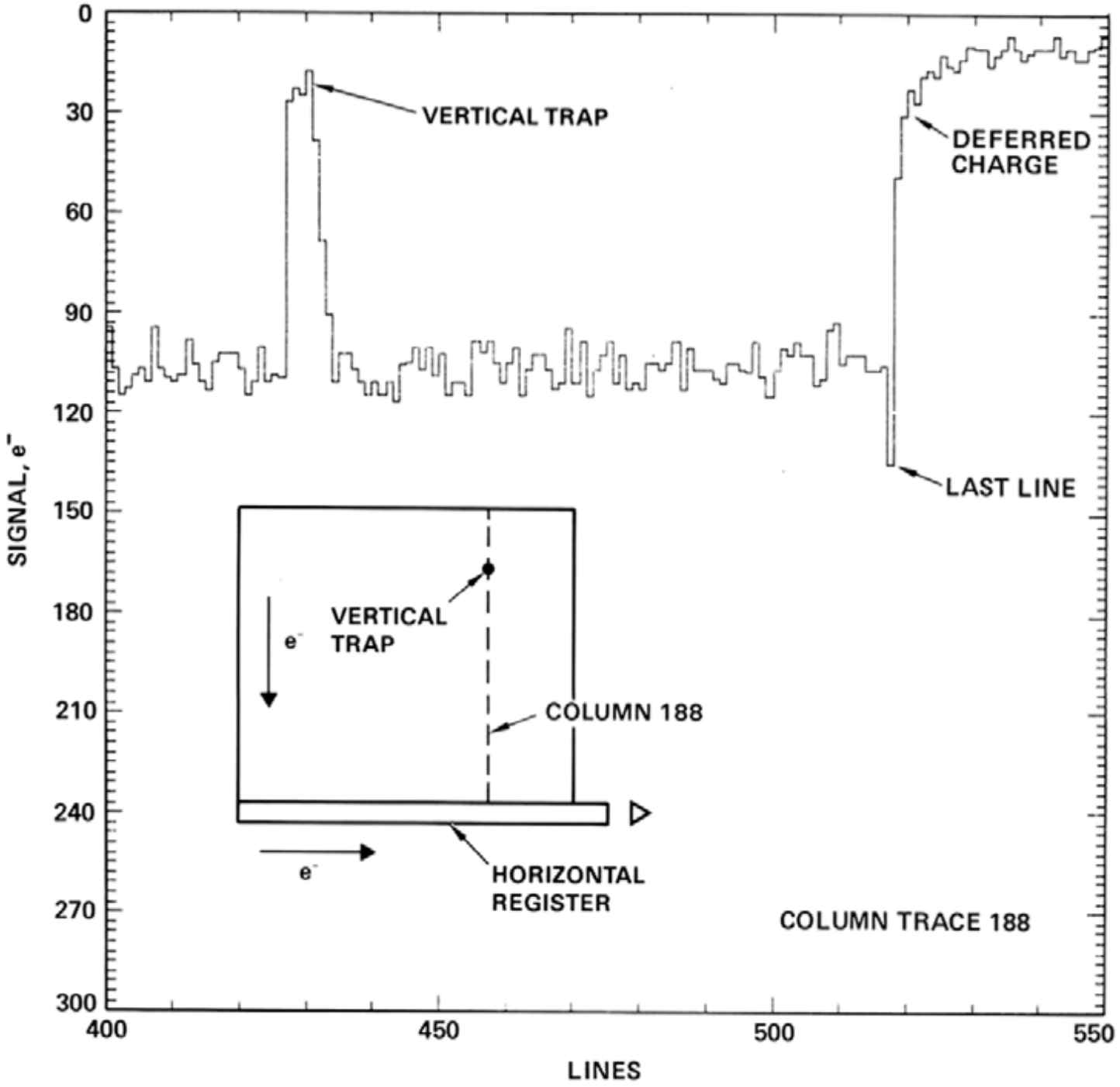
Q_d: Net deferred charge in the overscan.

Q: Charge on the last real pixel.

N: Number of pixels transferred.

Figure 8.10 illustrates an example of EPER under low light levels.

A plot of the signal along a particular column (column 188) of a CCD showing the loss of charge in a "trap".



8.4 Bad pixels and charge transfer efficiency

- Spurious potential pockets in now well-enough understood.
- isolated single-pixel traps or "pocket" randomly affect individual pixels, disrupting CTE on a local level.
- Some CCDs had many such pockets. These traps were localized to a specific level of the polysilicon electrode within a pixel.

e.g.) This problem affected Tektronix (SITe) CCDs

- Two clues:

- Boron diffusion: TI 800x800 CCDs showed no large single-pixel traps, leading to a discovery about boron diffusion. Boron, used to dope the p-type substrate, diffused through the n-type epitaxial layer during a high-temperature manufacturing phase. ("p+ epitaxial diffusion tail")

- Tek CCDs show little diffusion of boron. A key realization was that changing the insulating material from silicon dioxide (SiO_2) to an oxide-nitride (NO) double layer could solve the problem. This new material significantly reduced short-circuits between the polysilicon electrodes, improving the manufacturing yield.

→ Pinhole created by surface contamination, allowing the nitride to diffuse through the oxide layer into the n-type semiconductor. Different insulator material caused slight variations in electric potential within the semiconductor at the tiny location.

8.4 Bad pixels and charge transfer efficiency

- Despite solving other issues, it is traps in the bulk silicon crystal that limit CTE in CCDs.
- The quality of manufactured semiconductor silicon has improved significantly over time, and will probably continue to do so.
- Global CTE performance of selected CCDs is believed to be limited by bulk traps to a level of 0.9999995 per pixel transfer, also called "six nines five" per pixel transfer

→ only 3 electrons out of a total of 10,000 electrons are deferred for 512 pixels.

8.4 NOISE SOURCES

- CCDs create images by transferring charge packets from each pixel, with the amount of charge proportional to the light hitting that pixel.
- When each charge packet reaches the output amplifier (a field-effect transistor), it causes a change in voltage proportional to the charge.
- The voltage change $V = Q/C$, where Q is the charge and C is the output node.
- In early CCDs, the output capacitance was around C ~ 0.6 picofarads (pF), yielding a voltage change of 0.25 microvolts (μV) per electron. In modern CCDs, capacitance is <0.1 pF, resulting > 16 μV/electron.
- Some Kodak CCDs, MOSFET give 15 μV/electron,

→ The overall noise under slow-scan conditions is greater than 10 electrons because other noise sources become larger as the size of the MOSFET gets smaller.

8.4 NOISE SOURCES

- The ideal situation is to ensure that the noise performance of a CCD camera is limited only by the output transistor and not affected by other electronic components.
- To achieve minimal noise, it is crucial to identify and minimize the various sources of unwanted electronic noise associated with the CCD.
- This minimal noise level is referred to as the "readout noise" (R), usually expressed as the root-mean-square noise in electrons.
- Potential sources of unwanted electronic noise:

- Background charge associated with fat-zero offsets
- transfer loss fluctuations
- reset or kTC noise
- MOSFET noise
- fast interface state noise

8.4 NOISE SOURCES

- Background charge associated with fat-zero offsets

When pre-flash is used to aid transfer efficiency or eliminate charge skimming:

noise = SQRT(Total number of charges in a pixel)

- transfer loss fluctuations

- In charge transfer, a fraction of charges are left, and this fraction may fluctuate

→ add some " transfer noise" $\sigma_{\mathrm{tr}} = \sqrt{2\varepsilon n N_0}$

where ε = 1- CTE, n: number of transfers, N0: number of original charges,

Fator of 2: Poisson distributed noise happen twice when trapped and released.

- For surface-channel CCD ~ 70 electrons
- Typically, ten times smaller for buried-channel CCDs and astronomical light levels

8.4 NOISE SOURCES

- reset noise (kTC noise): √(kTC)/e → 284√(C) (at T = 150 [K], C ~ pF)

→ dominant source in most cases

- one-over-f noise: noise that varies roughly 1/frequency

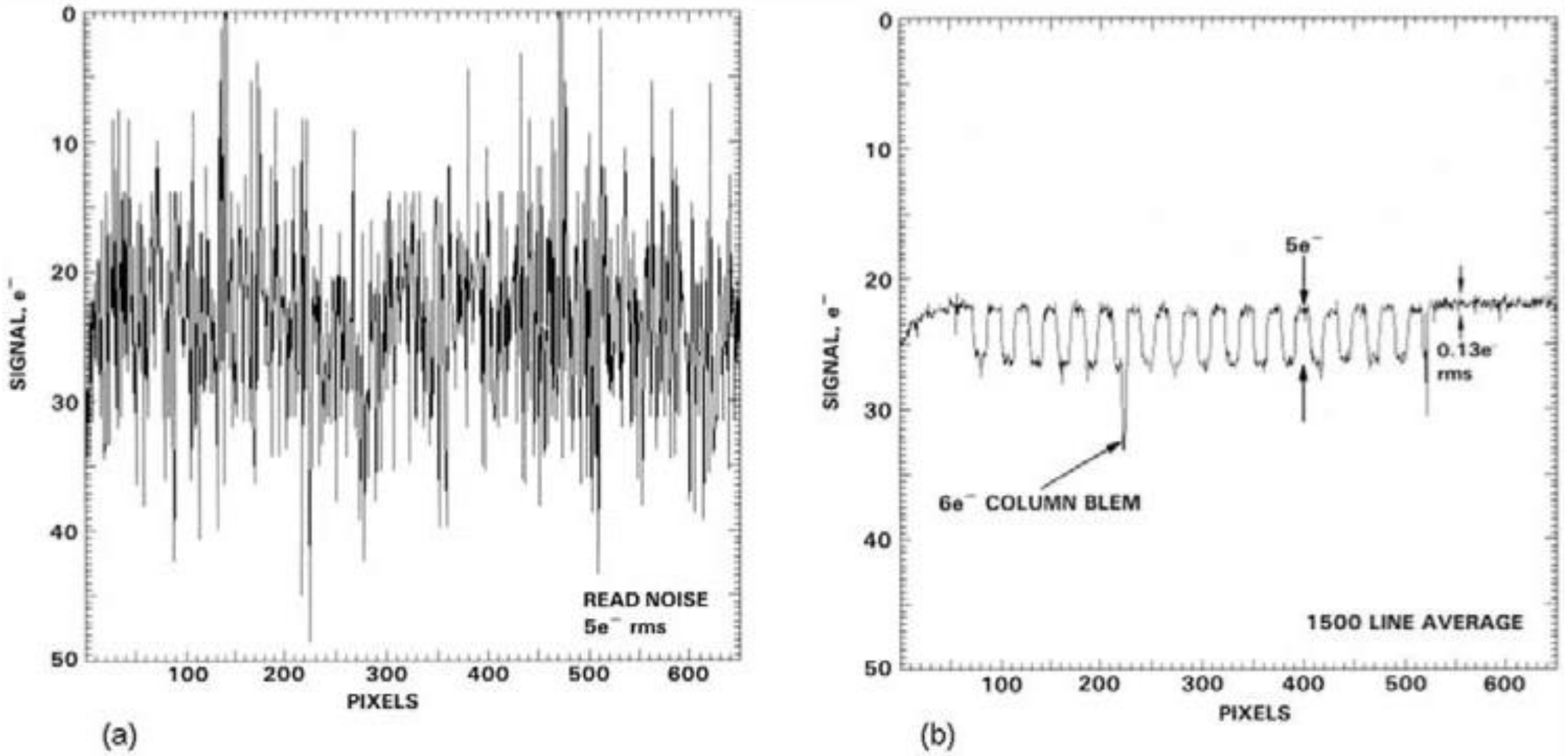
→ usually small (~ few electrons) by good manufacture

- fast interface state noise:

$$\sigma_{ss} = \sqrt{2kTnN_{ss}A}$$

- Traps that absorb and release the charges on very short time scales, causing fluctuation in the charge in any pixel = "fast interface states"
- k: Boltzmann's constant, T: absolute temperature, n: total number of transfers,
- Nss: surface density of traps, A: surface area
- Serious for surface-channel CCDs, but is quite small (5 electrons or less) for good buried-channel CCDs

- Devices are now routinely made with a readout noise of less than 5 electrons, thanks to every scientist and engineer who worked for CCD tech.



A single raw trace of the signal from a Loral CCD at the five-electron level. Embedded in the noisy trace is an unseen 5e peak-to-peak square-wave pattern. (b) After 1,500 lines have been averaged the random noise is only 0.13e as seen in the overscan region. A 6e column blemish (BLEM) has also emerged. Credit: Jim Janesick.

8.6 SIGNAL PROCESSING AND DIGITIZATION

- Correlated Double-Sampling (CDS): important technique used in CCD signal processing.

- As each charge packet reaches the output node, it causes a voltage change that needs to be amplified and digitized by an analog-to-digital (A/D) converter.

- The conversion process takes time, hence the term "slow-scan."

- A high degree of accuracy is necessary, achievable with a 16-bit A/D converter. This converter divides a specific voltage range (e.g., 10 volts) into 65,536 (2^16) parts, making each voltage interval about 152.5 uV.

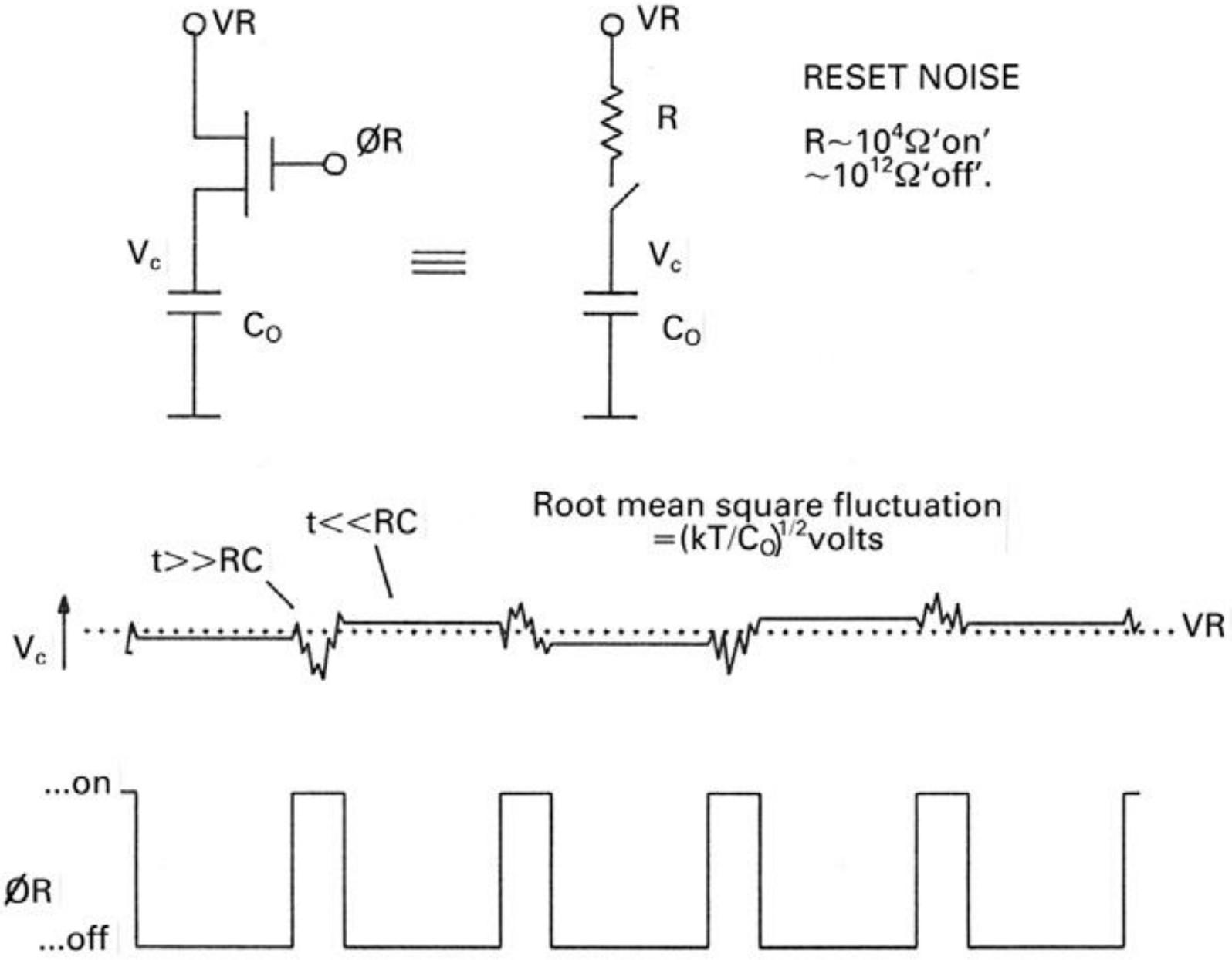
→ The A/D circuit matches up the actual voltage to the nearest number on the scale of 0 — 65,535.

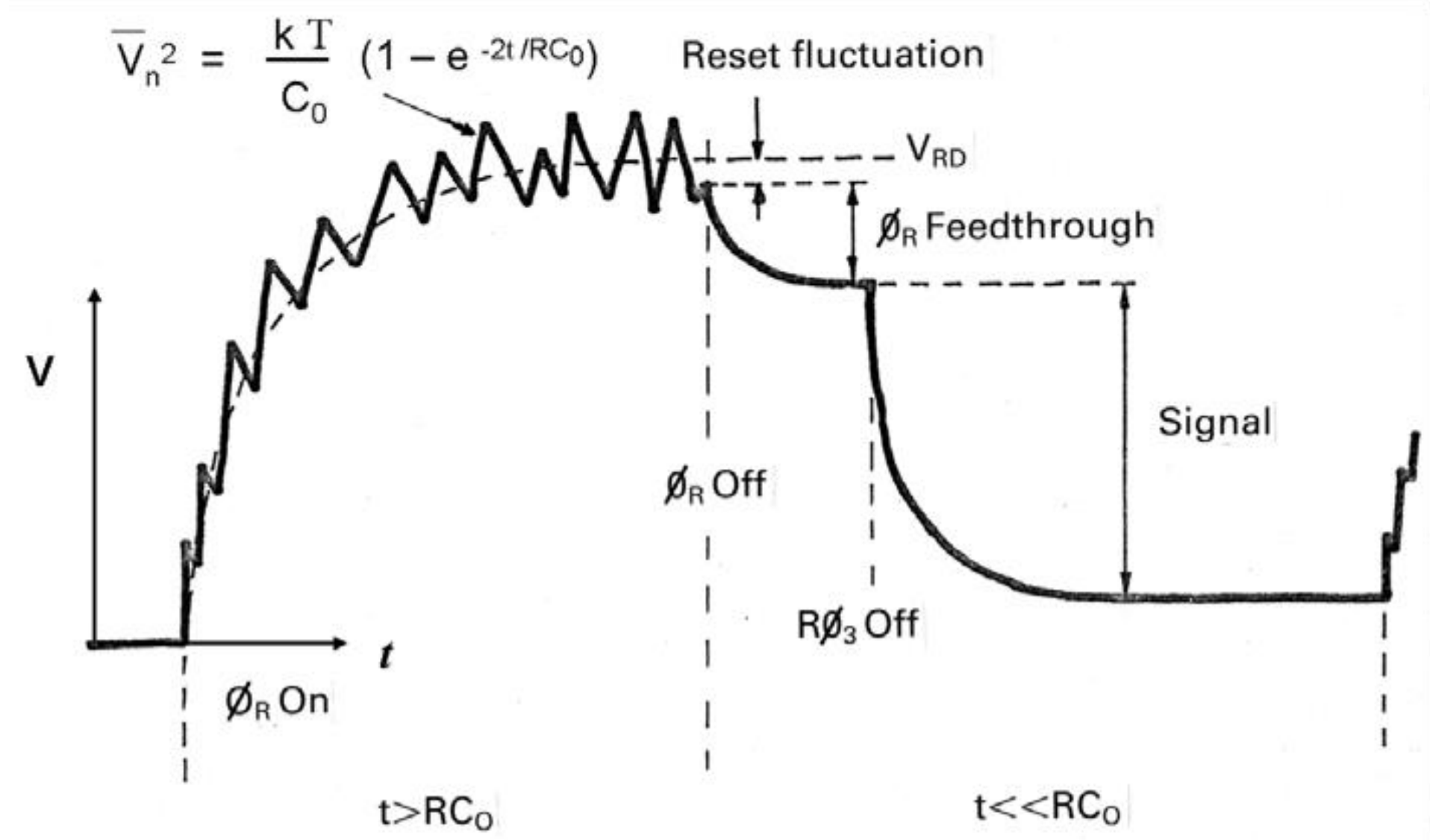
- To measure the voltage of each charge packet accurately, a reference voltage is needed. While ground could serve as the reference, it's important to reset the output capacitance to a nominal value with each readout cycle to avoid drifting from the ideal operating point of the MOSFET.

- Instead, the output capacitor can be recharged to a fixed voltage by briefly pulsing the gate of a reset transistor. This effectively acts like a switch to allow current from a power supply to charge the node to the desired voltage.

- When the reset pulse ends, the reset transistor turns off, isolating the output for the next charge transfer. The capacitor charges exponentially, starting steeply and then leveling off.

An equivalent "switch" circuit to explain the operation of the reset transistor. The resistance, and therefore the RC time constant, is very different between off and on states.





The charging profile of the output of a CCD when the reset transistor turns on, following an exponential charging curve. The curve is "noisy" but when the reset pulse disappears the last value of the signal becomes frozen.

8.6 SIGNAL PROCESSING AND DIGITIZATION

- Due to random thermal agitation of electrons, there's always a small uncertainty in the final voltage value after the reset process.

- Formula for Reset Noise: $$\text{reset noise} = \sqrt{\frac{kT}{C}} \text{ volts or } \frac{\sqrt{kTC}}{e} \text{ electrons}$$

- Where, k is Boltzmann's constant (1.38×10^{-23} J/K), T is the temperature in Kelvin, C is the node capacitance in farads.
- If the node capacitance C is expressed in picofarads, the reset noise (both in terms of voltage and electrons) becomes a significant factor. Smaller capacitance helps reduce this noise.
- $400\sqrt{(C)}$ at room temperature, $250\sqrt{(C)}$ at 120 K

→ < 80 electrons noise which greatly exceeds readout noise of MOSFET alone.

→ need to remove