Section 8.6.1- End of Section 8

McLean seminar
2024.10.18

Section 8.6.1 Correlated double-sampling

Correlated double-sampling (CDS)

1. Definition

- CDS is a widely used technique in CCD detectors to reduce or eliminate reset noise.
- Reset noise is the random fluctuation in voltage that occurs when the detector is reset after reading each pixel.

2. Key Concept

- Two voltage samples are taken per pixel: one before the charge packet is dumped and one after.
- The difference between these two samples effectively cancels out the reset noise, without needing to know the exact value of the reset voltage.

3. Why Important?

- CDS improves the signal quality by removing noise that could distort faint astronomical signals.

Section 8.6.1 Correlated double-sampling

Reset Noise and Its Removal in CDS

1. Reset Noise

- Occurs due to fluctuations in the final reset voltage, which can vary within the range of $(V_{\text{RESET}} - \sqrt{(kT/C)})$ to $(V_{\text{RESET}} + \sqrt{(kT/C)})$
- This noise results from thermal effects and the capacitor value in the CCD's output circuitry.

2. Solution

- After resetting, the voltage stabilizes (or "freezes") due to the very slow leakage of current through the reset transistor (the RC time constant is much longer than the interval between charge packets arriving).
- By taking two samples—one just before and one just after a charge packet is output—the same reset noise is present in both samples.
- Subtracting the two samples cancels out the noise, leaving just the signal from the charge packet.

Section 8.6.1 Correlated double-sampling

How CDS Works: Step-by-Step Process

1. Sampling Process

- **Before Charge Packet (Pre-Sample)**: Voltage is sampled by the A/D converter just before the charge packet is dumped.
- **After Charge Packet (Post-Sample)**: Voltage is sampled again after the charge has been added.
- **Difference Calculation**: The two samples are subtracted, removing the reset noise and isolating the charge packet's signal.

2. Why Effective?

- The reset noise is common to both samples (correlated), making it easy to eliminate by subtraction.

3. Diagram Reference

- Use Figure 8.14 to show how the CDS circuit is structured.

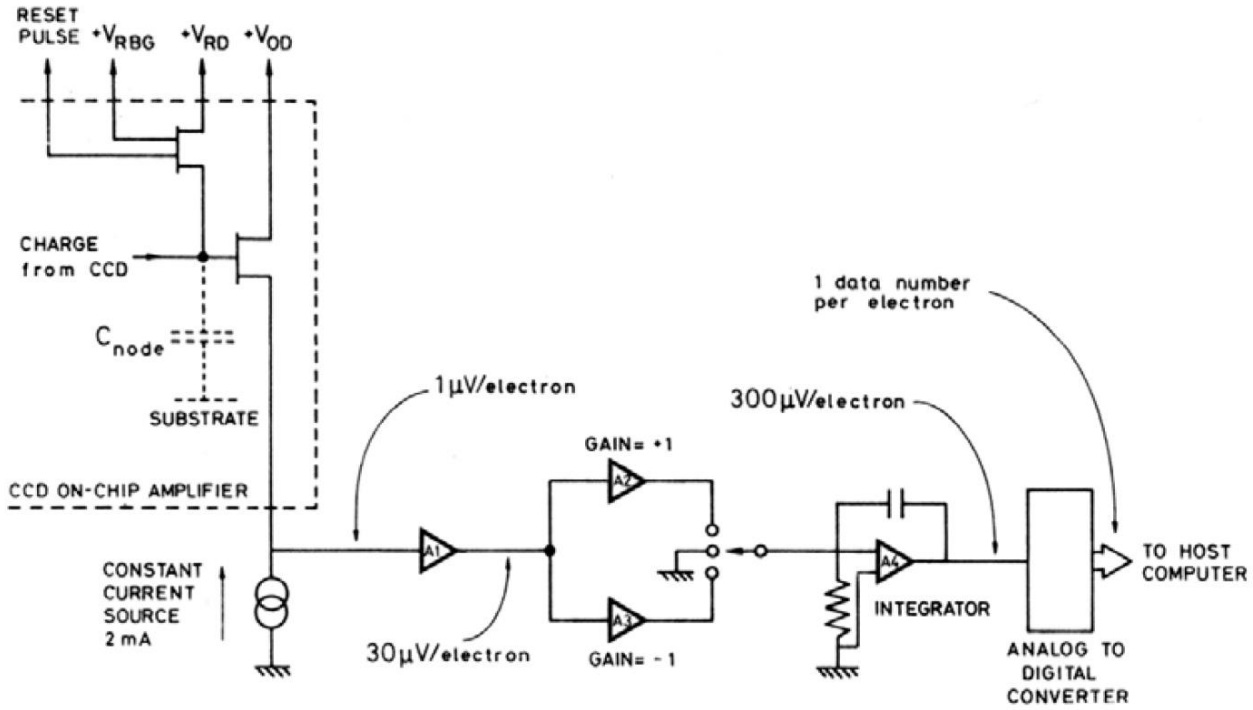

Figure 8.14. A block diagram of the principle of the correlated double-sampling (CDS) method of removing reset noise before the signal is digitized and sent to a computer. Credit: Craig Mackay.

Section 8.6.1 Correlated double-sampling

CDS Circuit Design and Components

1. Amplifiers
- The CDS circuit uses a series of amplifiers to process the signal from the CCD output.
- **Low-noise operational amplifier (A1)**: Amplifies the small voltage signal from the CCD output.
- **Integrating amplifier (A4)**: A capacitor in the feedback loop integrates the signal over time, reducing noise.

2. Three-position Switch
- **Ground**: Used to isolate the integrator.
- **Inverting Amplifier (×-1 gain)**: The reset level is integrated negatively onto the capacitor.
- **Non-inverting Amplifier (×1 gain)**: The reset + signal voltage is integrated positively onto the same capacitor.

3. Result: Only the true signal due to the charge packet remains, with the reset noise eliminated.

Section 8.6.1 Correlated double-sampling

Why Integration is Better Than Spot-Sampling

1. Advantages of Integration

- **Noise Smoothing**: Integration smoothes out high-frequency noise that would otherwise interfere with the signal.
- **1/f Noise**: Low-frequency noise (1/f noise) is also minimized, making the signal more accurate.

2. Schematic Operation

- During integration, the amplifier takes input from both the inverting and non-inverting paths for an equal amount of time.
- The integration ensures that only the real difference (the charge packet signal) remains.

Section 8.6.1 Correlated double-sampling

Importance of Amplifier Gain in CDS Systems

1. Amplifier Gain

- Amplifier gain determines how much the signal is amplified before it reaches the A/D converter. This is crucial for detecting weak signals, as too low a gain can result in the loss of important data, while too high a gain can lead to saturation.

2. Balancing Gain

- **Example**: For a CCD with a full well capacity of 500,000 electrons and a readout noise of 5 electrons:
    - Choosing a gain of 1 electron per DN (data number) results in a readout noise of 5 DN.
    - This would saturate the A/D at only 13% of the full well capacity.

- **Better Choice**: Use a gain of 5 electrons per DN, so the readout noise is 1 DN, allowing better use of the A/D range (up to 65% of the well capacity).

Section 8.6.1 Correlated double-sampling

Readout Noise and CDS Performance

1. Readout Noise

- Proportional to the sensitivity of the CCD's output node (μV/electron) and the filtered noise spectrum of the amplifier.

2. Effect of Integration Time

- The longer the integration period, the lower the noise. This continues until 1/f noise starts to dominate, at which point the benefits taper off.

Section 8.6.2 On-chip binning

Introduction to On-chip Binning

1. Definition

- On-chip binning combines multiple pixel charges into a single "superpixel" by summing their charge packets at the output node capacitor.

2. Purpose

- Reduces image resolution but improves signal-to-noise ratio.
- Particularly useful in applications where signal levels are low, such as faint astronomical objects.

How On-chip Binning Works

1. Vertical Binning

- Multiple rows are combined by skipping the horizontal clocking after vertical transfers.

2. Horizontal Binning

- Multiple pixels are combined by omitting the reset pulse between horizontal transfers.

-> The output image has fewer pixels, but each pixel contains more charge, resulting in a higher signal-to-noise ratio.

Section 8.6.2 On-chip binning

Applications of On-chip Binning

1. High-resolution Spectroscopy

- In instruments like echelle spectrometers, binning along the dispersion axis (parallel to the spectrum) can enhance the signal without compromising resolution.
- Binning across the dispersion axis (perpendicular) can significantly improve the signal-to-noise ratio in faint sources.

2. Variable Seeing Conditions

- In astronomy, on-chip binning is also useful for adjusting resolution to match atmospheric conditions.

Section 8.6.3 Overscanning and sub-arrays

What are Overscanning and Sub-Arrays?

1. Overscanning
- Technique where extra pixels beyond the CCD boundaries are read.
- Purpose: To obtain the bias level.
- Used to measure the "noise level" by reading pixels from the inactive area at the edge of the CCD sensor.

2. Sub-Arrays
- A method to read only a portion of the CCD to increase speed.
- Application: High-speed measurements for specific regions (e.g., star guiding).
- Helps reduce data processing time and focuses analysis on selected regions.

Section 8.7 Uniformity of response

Addressing Uniformity of CCD Response

CCDs often exhibit non-uniform response, even in flat-field illumination.

1. Causes of Non-Uniformity
- Pixel sensitivity variation: Different pixels respond to light at varying intensities.
- Defective pixels, blocked columns, dust: These defects can hinder accurate response.
- Non-linearity: Parts of the CCD may respond non-linearly to light intensity.

2. Solution
- Use flat-field calibration to remove the non-uniformity of the CCD.
- Corrects the relative sensitivity of each pixel using flat-field images for uniform results.

Section 8.7 Uniformity of response

Wavelength Dependency of CCD Response

1. CCD response by wavelength

- Photons of different wavelengths are absorbed at different depths in silicon
- Example: Short-wavelength light (UV) is absorbed near the surface, while long-wavelength light (IR) penetrates deeper.
- This causes color-dependent non-uniformity in how the CCD absorbs light

2. Solution

- Flat-fielding can be used to correct for this wavelength-dependent variance.

Section 8.8 UV Flashing and QE Pinning

UV Flashing and QE Pinning

1. UV Flashing

- A method to improve the quantum efficiency (QE) of CCDs.Uses UV flashing to fill trapping sites within the CCD.
- Effect: Reduces dark current and enhances efficiency, particularly in the blue and UV regions.

2. QE Pinning

- After UV flashing, the quantum efficiency is enhanced and pinned under certain conditions.

Enhancing Quantum Efficiency with Surface Treatments

1. Phosphor Coating

- Used to enhance CCD sensitivity to ultraviolet light.
- Example: Coatings like Coronene or Metachrome II increase UV sensitivity.

2. Additional Treatments

- Some CCDs may require exposure to UV light or chemical treatments to boost quantum efficiency.

Efficiency of Thinned and Backside-Illuminated CCDs

1. Thinned CCDs
- CCDs with reduced thickness to significantly improve quantum efficiency.
- Particularly effective for UV and near-infrared (NIR) regions.

2. Backside Illumination
- Light enters the CCD from the back, improving overall sensitivity.
- Issue: Can lead to interference fringes at long red wavelengths.

Section 8.9 Summary

Summary of CCD Technology

1. Key Technologies
- Overscanning, Sub-Arrays, flat-fielding, UV flashing, and other methods to optimize CCD performance.

2. Challenges
- Non-uniformity, interference fringes, and other issues can be resolved through careful calibration.

3. Future Outlook
- The advancement of thinned and backside-illuminated CCD technologies promises even higher efficiency.